PRELIMINARY LOGICAL DESIGN OF AN ELECTRONIC DESK CALCULATOR

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the Degree of Master of Technology

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SWAPAN KUMAR RAY
Indian Institute of Technology
Kanpur

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ABSTRACT

The content of this Thesis forms the preliminary work towards the Desk Calculator Project undertaken by the Electrical Engineering Department at the Indian Institute of Technology, Kanpur. Complete system and logic design, based on counter type arithmetic, of a small five-digit electronic desk calculator performing the operations of addition, subtraction, multiplication and division in the integer mode has been worked out. A comprehensive scheme for automatic decimal point adjustment has been developed and used for the design of a more sophisticated desk calculator having ten-digit capacity, operating in the floating point mode and performing the additional operations of accumulative multiplications.

ACKNOWLEDGEMENT

The author is deeply indebted to Dr. V. Rajaraman for his able guidance and abounding encouragement throughout the entire work. He also takes this opportunity to thank Dr. H.N. Mahabala and Dr. T.R. Viswanathan for making a few valuable suggestions.

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CHAPTER - I

1.1 INTRODUCTION:-

With the rapid growth of business and industry in the country, a need for automatic computing and calculating machines in carrying out the large volume of numerical computations is being felt. Consequently, there is a need for developing a fast, reliable and efficient automatic computing service- freeing the army of clerks from the repetitive and tiresome mental computations that are inherently slow, unreliable and a drudgery. With this background and with a realistic assessment of the state of industrial development in the country, it was felt that it would be a worthwhile project to design and develop an electronic desk calculator incorporating all the important features available in present day calculating machines, using indigenous components and at a moderate cost. The present work is intended to serve as a description of the scope, features, system and logic design as well as some of the important practical aspects like cost estimation, feasibility of being manufactured in India, etc. of the proposed electronic desk calculator.

1.2 BRIEF HISTORY OF DESK CALCULATORS:-

The human effort towards mechanisation of computations dates back to as early as the Sixth Century B.C., when people

in China started using "abacus" or counting frame, the first true calculating machine. The abacus, whose operation seems to be a development from the counting on the fingers, is still in use in many parts of the world and was probably the root of the decimal system. The decimal system is now almost universal and all desk calculators are decimal.

The first calculating machine similar to those we know today was the adding machine invented by Blaire Pascal in 1642. After about three decades, in 1671, G.W. Leibniz developed a calculator which for the first time achieved mechanisation of the process of multiplication and which is considered as the forerunner of all modern calculating machines. Finally, reliable calculating machines, the introduction of which was delayed by difficulties in manufacturing reliable mechanical components, became available for sale in the last decade of the Nineteenth Century. Since then the computing machines industry has witnessed a rapid and continuous development and today we find desk calculators and computers in hundres of makes and thousands of varieties.

1.3 COMPONENT PARTS OF A DESK CALCULATING MACHINE AND HOW IT WORKS:-

Most of the component parts listed here are common to all types of mechanical and electro-mechanical desk calculators but only a few of these are found in electronic desk calculators, the principle of operation of which is vastly different.

1.3.1 SETTING REGISTER (S.R.):-

This is the entry register in the machine, as it normally stores the number temporarily while the same is being entered. The Setting Register is classified into the following three types depending on the method of entry of the digits:

(A) Lever Type:

A lever sliding in a slot can occupy any one of specified ten positions numbered consecutively '0' through '9'

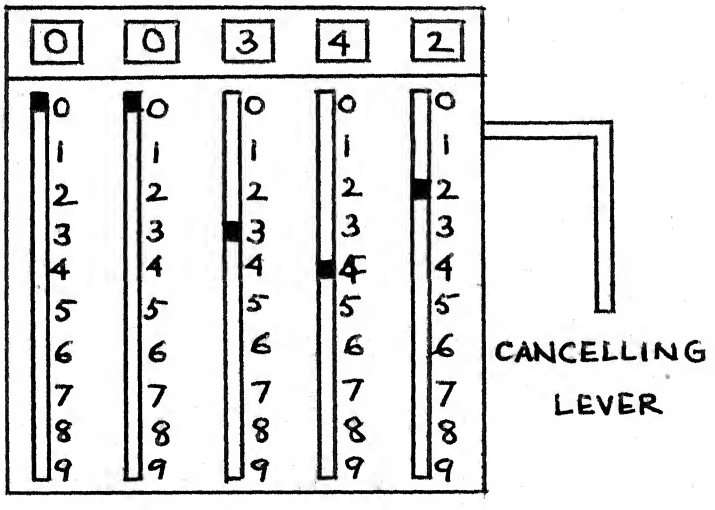


FIG. 1·1 A LEVER SETTING REGISTER

and the Setting Register consists of several such levers (equal to digit-capacity) placed side by side. The register is fitted with a cancelling lever which will return it to zero.

(B) Keyboard Type:

A column of ten keys numbered consecutively from '0' to '9' is available for each of the digit positions in S.R.

(i.e., 5 x 10 = 50 keys in all for a 5-digit S.R.). A

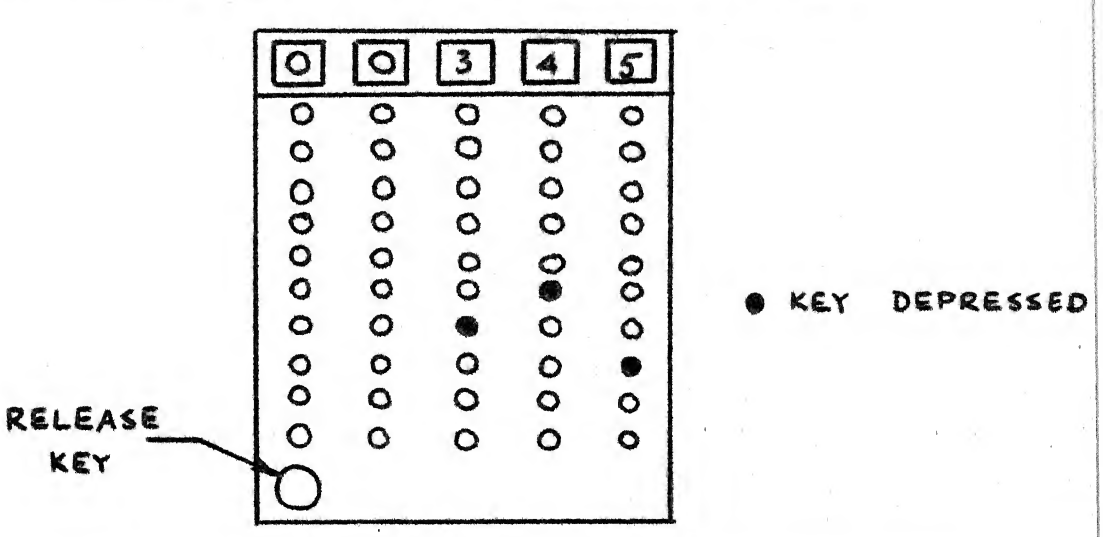


FIG. 1·2 A KEYBOARD SETTING REGISTER

cancelling key will return the whole register to zero.

(c) <u>Ten-Key Type</u>:

Only ten keys are available numbered '0' to '9'.

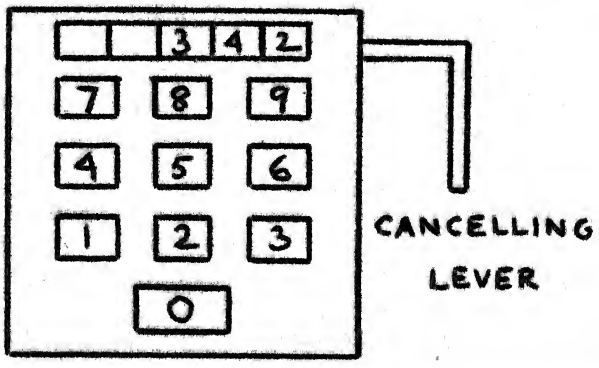


FIG. 1·3 A TEN-KEY SETTING REGISTER

These are depressed in succession starting from the most significant digit. The register will be fitted with a lever or key.

The number entered is displayed through special window in each of the above types of S.R.

1.3.2 PRODUCT REGISTER (P.R.):-

This is generally the largest-capacity register in the machine and is the most important of all as well. P.R. is provided with a cancelling key or lever and if the operating handle (described in Section 1.3.4) is rotated once forwards, the number set in S.R. is transferred to P.R.

1.3.3 MULTIPLIER REGISTER (M.R.):-

This register counts the number of turns of the operating handle and is provided with a cancelling key or lever. It counts up or down depending on whether the Forward or Reverse Lever (described in Section 1.3.6) is set to + or -.

The P.R. is always provided with Tens Transmission while in M.R. it is usually, but not necessarily, provided.

1.3.4 OPERATING HANDLE (O.H.):-

O.H. is found coupled with S.R. in manually operated desk calculators and can be rotated forwards or backwards, but the rotation must be complete. On electrically operated

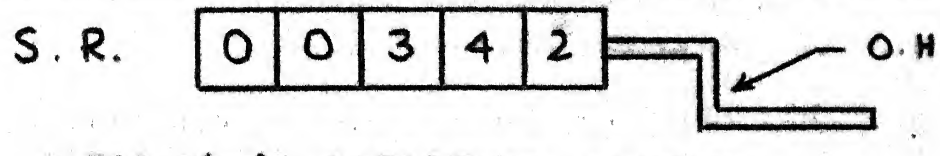


FIG. 1·4 OPERATING HANDLE

machines, the O.H. is replaced by Plus and Minus Bars.

1.3.5 POSITION INDICATOR (P.I.):-

In non-electronic calculators, S.R. (or P.R. or M.R.)

moves to and fro relative to P.R. (or M.R. or S.R.). The P.I. is an arrow or mark which indicates the position of a window

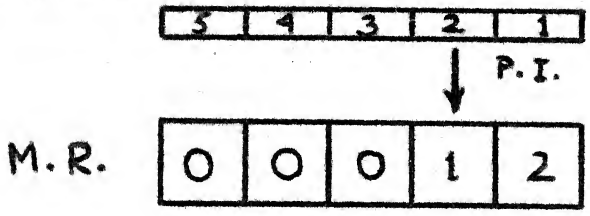


FIG. 1·5 POSITION INDICATOR

in M.R. The M.R. counts the turns of the O.H. but the position where the counting takes place is variable and is indicated by P.I.

1.3.6 FORWARD OR REVERSE LEVER (±):-

Although not often found on hand-operated machines, this device is found frequently on electric calculators. It is set at '+' for positive and '-' for negative entries in M.R.

1.3.7 DECIMAL POINT MARKERS (D.P.M.):-

These are sliding markers found in each register.

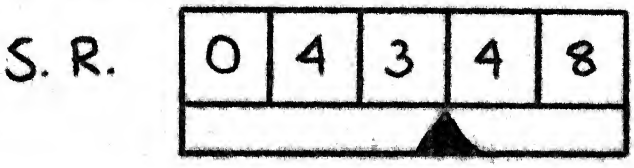


FIG. 1·6 DECIMAL POINT MARKER

1.3.8 CANCELLING LEVERS OR KEYS:-

Each register on all modern calculating machines is fitted with a lever or key which returns the register to zero. An additional lever is normally provided to cancel all the

registers together (see FIGS. 1.1, 1.2 and 1.3).

1.3.9 STORAGE REGISTER (ST. R.):-

Storage or Memory Registers are used either for storing numbers which are ~~registered~~ required frequently or for the storage of an intermediate result which is used later at the appropriate point of calculation. Storage registers are very useful and ideally should be (i) linked with any of the three basic registers, (ii) capable of retaining the content after transfer and (iii) also to accumulate totals.

1.3.10 MULTIPLIER SETTING REGISTER (M.S.R.):-

In some machines (especially keyboard type), for automatic multiplication, an extra register M.S.R. is provided to take in and store the multiplier. This is very much useful for multiplication involving a constant multiplier and M.S.R., like the other registers, is also fitted with a cancelling key.

1.4 TYPES OF DESK CALCULATING MACHINES:-

1.4.1 ADDING MACHINES:-

Adding machines are Desk Calculators used extensively for accounting purposes. They are advantageous for addition and subtraction but not much suited for multiplication and division.

Basically an adding machine consists of a S.R., linked with a Totals Register (T.R.) which as different from a P.R., has

the same capacity as S.R. and is immovable with respect to it. A few of the commonly used varieties of adding machines are described below:

(A) Key-driven Adding Machines:

This type of machine has a keyboard setting register and the desired number is directly and immediately added into the Totals Register just by pressing the corresponding keys.

(B) Adding Listing Machines:

Here the numbers are entered by keyboard into S.R., and by operating the machine once (by O.H. ~~only~~ or by Plus or Minus Bars) the number is transferred to T.R. Simultaneously the number is printed on a roll of paper so that a list of the numbers contributing to the total in T.R. appears in printed form. This type of machines can be manually or electrically operated.

(C) Accounting Machines:

The simplest accounting machines are cash registers, and in addition to adding, subtracting and listing, receipts for customers can be provided; also a limited number of special keys are available which will print additional relevant word informations alongside the list of numbers.

1.4.2 MANUALLY OPERATED DESK CALCULATORS:-

These machines contain all the basic features of a calculating machine, namely, S.R., P.R., M.R. and P.I., and are operated by O.H., which can be rotated forwards or backwards.

The most important special features to be found on hand-operated machines are the "back transfer" (transfer of the content of P.R. to S.R. or M.S.R.) and "storage register".

1.4.3 ELECTRICALLY OPERATED, SEMI-AUTOMATIC DESK CALCULATORS:-

The main spindle in these machines is driven by an electric motor. The rotation of the motor is governed by two keys- "Plus Bar" (forward rotation) and "Minus Bar" (reverse rotation). These machines are termed semi-automatic because the process of division is, almost invariably, completely automatic.

1.4.4 ELECTRICALLY OPERATED, FULLY AUTOMATIC DESK CALCULATORS:-

(A) Automatic Addition and Subtraction:

Automatic machines are provided with Plus and Minus Bars together with a Repeat-Non Repeat Key. In the Non-Repeat position, a number in S.R. is transferred destructively into P.R. on the depressing of the Plus or Minus Bar.

(B) Automatic Multiplication- Live Key Multiplier:

These machines are fitted with a column of "Live Keys". The multiplicand is entered into S.R. as usual and the multiplier is fed through the live keyboard, a digit at a time; as each digit is entered the machine carries out the corresponding multiplication and moves one position so that when the multiplier has been entered, M.R. records the value of the multiplier and the product appears in P.R.

(C) Automatic Multiplication - Double Keyboard:

This uses a separate group of ten keys, usually arranged like a ten-key setting register, called M.S.R. The multiplicand is entered into S.R. and the multiplier into M.S.R. When a "Multiply" key is depressed, the multiplication is done automatically.

(D) Automatic Multiplication - Single Keyboard:

This appears to be the most popular system. The multiplier is first entered into S.R., and by depressing a key (often marked "X") it is transferred to a separate register (say M.S.R.). The multiplicand is entered next, also into S.R., and by depressing a key (often marked "="), the two numbers are multiplied and the result is stored in P.R.

In all forms of automatic multiplication, positive or negative multiplication is always possible, and totals in P.R. may be accumulated, if required.

(E) Automatic Division:

The dividend is entered into S.R. and by depressing a "Dividend Entry" Key, it is transferred automatically to the selected position in P.R. The division is entered next into the S.R. and depression of the "Divide" Key causes the machine first to line up and then to divide, the quotient appearing in M.R.

(F) Special Features:

(a) Back Transfer:

This is transfer of the contents of P.R. into S.R.

or M.S.R. and has two main advantages, namely

(i) Negative numbers displayed as complements in P.R. can be transferred automatically to their correct numerical value [See Section 2.4 B - Case (ii)] .

(ii) The process of "chain multiplication" is simplified.

(b) Automatic Squaring and Extraction of Square Root:

Both of these operations, particularly useful in statistics, can be performed by depressing the corresponding keys.

(c) Number of Products:

If a machine is being used to accumulate sums of products, a device is available on some machines which will record the number of products that have been entered.

(d) Storage:

It has already been described in Section 1.3.9.

1.4.5 PRINTING CALCULATORS:-

Introduced recently, these automatic electrically operated desk calculators have storage and transfer facilities and in addition they print the results in a manner similar to adding listing machines.

1.4.6 ELECTRONIC DESK CALCULATORS:-

From the operator's point of view these are similar to automatic electrically operated desk calculators but the

operations are done at electronic speed and these machines normally have electronic display systems.

1.5 PRESENT DAY DESK CALCULATORS:-

After the introduction of the first modern desk calculator in the last decade of the last Century, thousands of different types of desk calculators manufactured by hundreds of manufacturing companies all over the world have been developed and offered for sale. A few of the notable and popular models are listed below.

1. Monroe-Educator:

   Keyboard setting register, hand operated, capacity: 7 x 7 x 14

   (capacity of a desk calculating machine is expressed as: digit capacity of S.R. x digit capacity of M.R. x digit capacity of P.R.).

2. Brunsviga- Model B.20:

   Lever type S.R., hand operated, with transfer, capacity: 12 x 11 x 20.

   S.R. and M.R. are fixed and P.R. is movable.

3. Curta- Model II:

   Lever setting register, hand operated, capacity: 11 x 8 x 15.

4. Facit- Model C.M. 2-16:

   Ten key setting register, hand operated, with transfer, capacity: 11 x 9 x 16.

5. Monroe- Model 88N-213:

Keyboard S.R., fully automatic single keyboard, double P.R., double M.R., with transfer, capacity: 10 x 11 x 21.

6. Diehl- Model V.S.R.:

Keyboard S.R., fully automatic single keyboard, with transfer and storage, capacity: 9 x 9 x 18.

7. Olympia- Model RA-16:

Ten key S.R., fully automatic single keyboard, with transfer and storage, capacity: 8 x 8 x 16. The S.R. is fixed while M.R. and P.R. are located together on a moving carriage.

8. Facit- Model CI-13:

Ten key S.R., manually operated, P.R. and M.R. are fixed and S.R. is movable, capacity: 9 x 8 x 13 (weight 14½ lbs).

9. Monroe- 6F:

Keyboard S.R., electrically operated, capacity: 10 x 10 x 20.

10. Wang- Model 300:

Electronic calculator, Ten key S.R., automatic floating print and sign, electronic display, capacity: 10 x 10 x 10 (plus sign and decimal point).

According to the information received by the author, only one type of desk calculator, Facit C1-13, is made in India while a few imported models are available for sale from companies like Blue Star Company, Electronic Enterprises and others.

1.6 WHY ELECTRONIC WAS DECIDED UPON - ITS ADVANTAGES AND DISADVANTAGES:-

Admittedly, unlike as in many industrially advanced countries, in India Electronics has not so far been able to play a significant role in the growth and nourishment of industries; but there are unmistakeably clear signs of the increasing importance of electronics. Consequently, in spite of the fact that an electronic desk calculator does not compete at par with its mechanical counterpart in respect of cost, its choice prevailed because of the following advantages and relevant considerations.

(i) The purpose of designing and developing a desk calculator that can be manufactured indigenously is to help the country's import substitution scheme. Although it was only natural to think first of mechanical calculators which are so common, yet the idea failed to find favour because mechanical calculators a) need expensive jigs and fixtures together with high precision machining and parts and b) call for a regular maintenance like oiling, cleaning, etc. and frequent repair, the latter needing attention of an expert machinist. On the other hand, electronic calculators are fairly easy to fabricate once the machine is designed and it was felt that the fast developing electronics industry can do the job confidently with the technical knowhow already available in the country.

(ii) Electronic calculators are extremely fast in doing calculations (computations are done at electronic speed, although the total time saving is not much because a considerable portion of time is taken up by the process of entering data), highly reliable, pretty compact and noiseless.

(iii) Electronic models have proved very popular because of many a convenience to the operator (e.g., easy reading of large digit electronic display system, lightness, etc.) and many an extra feature like increased transfer and storage facilities.

(iv) One useful feature of electronic calculators is that several consoles, which may be far removed from one another, can be connected to a single electronic package (processing unit). This can effect substantial savings in the overall cost and may prove a boon to big offices.

(v) In mechanical calculators, the decimal point has to be taken care of by the operator himself which presents some difficulties, but an electronic desk calculator may be designed with floating point arithmetic.

(vi) Finally, the cost which seems to be a bit high at the present moment, is sure to come down with the development of integrated circuit techniques in India.

CHAPTER - II

2.1 SPECIFICATIONS OF THE PROPOSED SMALL MACHINE:-

In this chapter, an attempt is made to design a small desk calculating machine to carry out the four fundamental operations, viz., addition, subtraction, multiplication and division, with no floating point (i.e., integer mode operation only). The machine will have a capacity: 5 x 5 x 5 and an automatic display system. No printing facility is being envisaged at the moment.

2.2 THE DIFFERENT REGISTERS NEEDED:-

In order to carry out the desired single operations, only three registers are needed; they are:

1. SETTING REGISTER (S.R.) - 5 digits capacity
2. PRODUCT REGISTER (P.R.) - Do
3. MULTIPLIER SETTING REGISTER (M.S.R.) - Do

2.3 A BRIEF OUTLINE OF THE DISPLAY SYSTEM:-

The best possible means of providing output of a desk calculator is the visual display. In mechanical calculators the registers are directly displayed through respective windows, all at a time and without any extra expense. But this not being possible in electronic calculators, separate display system has to be provided and in order to

limit the cost, instead of using one display unit per each register, only a central display unit will be arranged. In the course of a particular operation, only the desired information is displayed at each step of operation automatically.

All the relevant details about the display system to be used will be discussed in Chapter-III.

2.4 SEQUENCE OF INDEXING AND OUTLINE OF CORRESPONDING MACHINE FUNCTIONS FOR DIFFERENT OPERATIONS:-

A. ADDITION:

Ex. 72 + 2531 =

1. PRESS "CLEAR ALL" - The entire machine is cleared and the display system is turned on.
2. INDEX 72 - 72 is entered into S.R. - S.R. is displayed.
3. PRESS "+" - The content of S.R. (i.e., 72) is added to the content of P.R. (i.e., 0) - S.R. is cleared - P.R., containing (0 + 72) i.e., 72, is displayed.
4. INDEX 2531 - 2531 is entered into S.R. - S.R. is displayed.
5. PRESS "+" - The content of S.R. (i.e., 2531) is added to the content of P.R. (i.e., 72) - S.R. is cleared - P.R., containing (72 + 2531) i.e. 2603, is displayed.

B. SUBTRACTION:

In the process of subtraction, two distinct cases arise, viz.

(i) subtraction of a smaller number from a greater number, giving rise to a positive difference and (ii) subtraction of a larger number from a smaller number, giving rise to a negative difference in the complement form (ten's complement: e.g., -351 in complement form will be 99649); both these cases will be considered with appropriate examples.

CASE (i) : Ex. 2531 - 72 =

1. PRESS "CLEAR ALL" - The entire machine is cleared and the display system is turned on.
2. INDEX 2531 - 2531 is entered into S.R. - S.R. is displayed.
3. PRESS "+" - The content of S.R. (i.e., 2531) is added to the content of P.R. (i.e., 0) - S.R. is cleared- P.R., containing (0 + 2531) i.e. 2531, is displayed.
4. INDEX 72 - 72 is entered into S.R. - S.R. is displayed.
5. PRESS "-" - The content of S.R. (i.e. 72) is subtracted from the content of P.R. (i.e. 2531) - S.R. is cleared- P.R., containing (2531 - 72) i.e. 2459, is displayed.

CASE (ii) : Ex. 72 - 2531 =

Same sequence as in CASE (i) is followed, viz.

1. PRESS "CLEAR ALL"
2. INDEX 72
3. PRESS "+"
4. INDEX 2531
5. PRESS "-"

} Corresponding functions have already been explained under under CASE (i).

Now, the subtrahend being greater than the minuend, P.R. displays the negative result in the complement form (i.e., 97541). This is indicated by an amber lamp.

In order to get the result in the normal form, i.e. -2459, an additional key has to be pressed.

6. PRESS "RESTORE" - The content of P.R. (i.e., 97541) is read into S.R. - P.R. is cleared - the content of S.R. (i.e., 97541) is subtracted from the content of P.R. (i.e., 0) - S.R. is cleared - P.R., containing the result in the normal form (i.e., 2459), is displayed with a negative sign.

(The above method of restoring is based upon the simple fact that double complementation of a number (i.e., taking the complement of a number in the complement form) gives back the original number).

C. MULTIPLICATION:

Ex. 72 x 251 =

1. PRESS "CLEAR ALL" - The entire machine is cleared and the display system is turned on.
2. INDEX 72 - 72 is entered into S.R. - S.R. is displayed.
3. PRESS "X" - 72 is retained undisturbed in S.R. and displayed - M.S.R. is made ready to accept the next entry.
4. INDEX 251 - 251 is entered into M.S.R. - M.S.R. is

displayed.

5. PRESS "=" - The multiplication takes place and the product is stored in P.R. - S.R. and M.S.R. are cleared - P.R. is displayed.

D. DIVISION:

Since no floating point is being used, obviously the dividend must be greater than the divisor and both the quotient as well as the remainder are of interest.

i.e., quotient = 360

Ex. $8295 \div 23 = 360\frac{15}{23}$ remainder = 15

1. PRESS "CLEAR ALL" - The entire machine is cleared and the display system is turned on.
2. INDEX 8295 - 8295 is entered into S.R. - S.R. is displayed.
3. PRESS "÷" - The content of S.R. (i.e., 8295) is added to the content of P.R. (i.e., 0) - S.R. is cleared - P.R., containing (0 + 8295) i.e. 8295, is displayed.
4. INDEX 23 - 23 is entered into S.R. - S.R. is displayed.
5. PRESS "÷" - The division takes place - the quotient is stored in M.S.R. and the remainder is left in P.R. - S.R. is cleared - M.S.R. is displayed.
6. PRESS "REMAINDER" - P.R., containing the remainder, is displayed.

2.5 LIST OF THE DIFFERENT KEYS, SWITCHES, INDICATORS, ETC. TO BE FOUND ON THE CONSOLE:-

SERIAL NO.	DESCRIPTION	NO. OF PIECES
1.	ON/OFF SWITCH	1
2.	CLEAR ALL KEY	1
3.	CLEAR S.R. KEY	1
4.	CLEAR M.S.R. KEY	1
5.	NUMERALS KEYS	10
6.	+, −, x, ÷ KEYS	4
7.	=, ≠ KEYS	2
8.	RESTORE KEY	1
9.	REMAINDER KEY	1
10.	NIXIE TUBES -NUMERIC	5
11.	NIXIE TUBES -SIGN	1
12.	COMPLEMENT FORM INDICATING AMBER LAMP	1
13.	OVERFLOW INDICATING RED LAMP	1
14.	RED LAMP INDICATING WHETHER POWER IS ON OR OFF	1

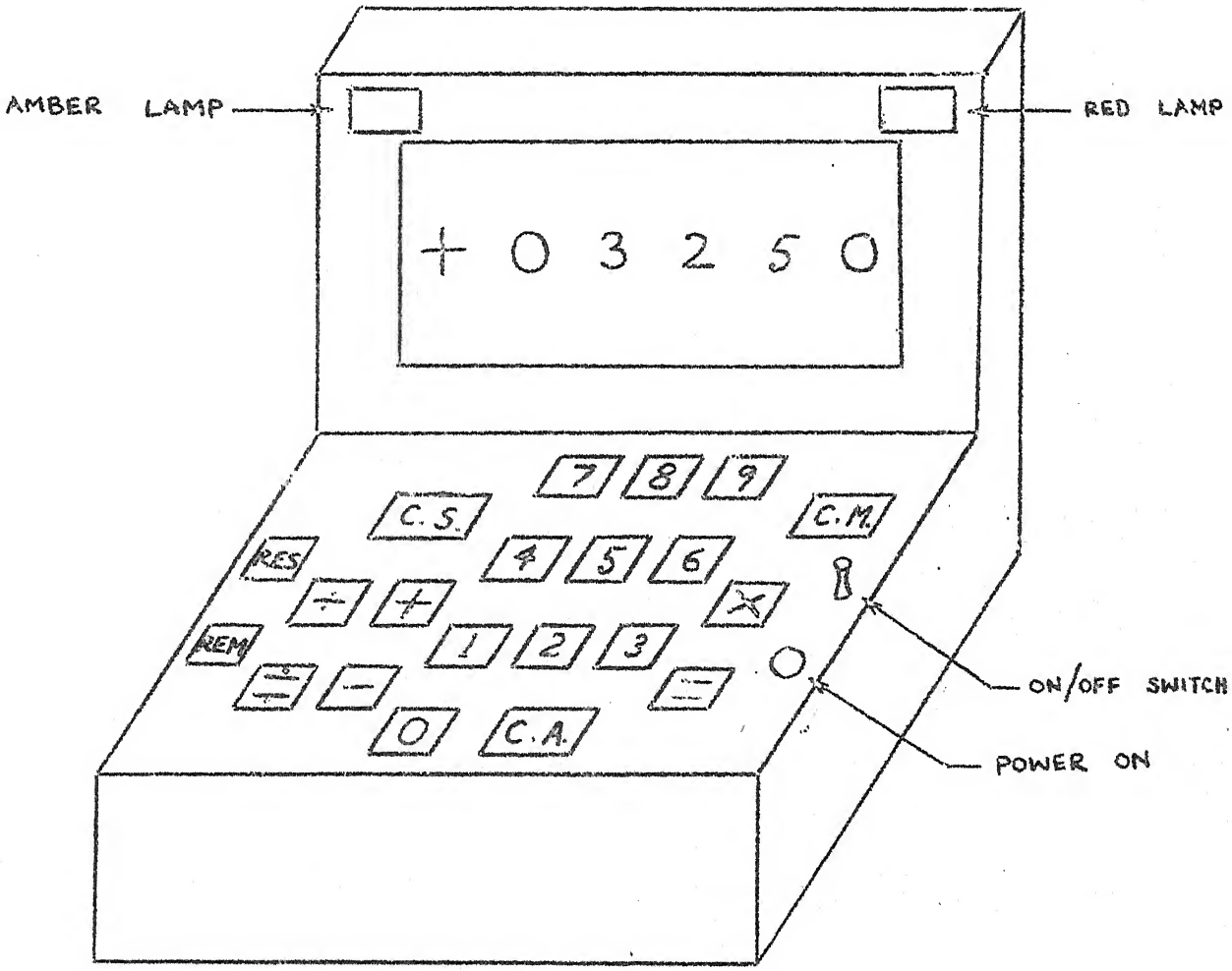


FIG. 2·1

A VIEW OF THE DESK CALCULATOR

CHAPTER - III

3.1 TYPE OF ARITHMETIC UNIT:-

The kind of arithmetic unit normally employed in digital computers is fairly complex and calls for a fast memory unit and a complicated control system; yet its use is economic and advantageous with stored programme operation and for large volume of information. But for desk calculators, where the inputs are fed directly and only four basic operations involving much lesser amount of information are needed, use of computer type arithmetic is not profitable. Instead, a counter type arithmetic looks to be fairly straightforward, most suitable, extremely simple and in all probability, less expensive. It can easily incorporate the simple function of counting up and down, shifting left and right and reading in- the only important functions necessary for carrying out the four fundamental operations of addition, subtraction, multiplication and division in a desk calculator.

3.2 CODING:-

Since the desk calculators use direct input and output in decimal number system, whereas no electronic machine normally operates internally on pure decimal number system (reasons are manifold, e.g., difficulties in achieving the hardware, less reliability, etc.), the necessity of using a

number system that is different from decimal, as the machine language, is obvious. Also because use of a memory unit is not being contemplated, no other number system (e.g., pure binary, octal, duo-decimal, etc. - which will need storage before being converted from decimal) can be used except a "binary coded decimal" number system that is suitable for direct and instantaneous conversion.

Again, unlike as in digital computers, in the present machine 9's complementation of numbers will not be needed to facilitate subtractions as a counter-type arithmetic has been proposed. Hence the use of any self-complementing code like Excess-3 or 2-4-2-1 will only present inconvenience. Thus as no special facilities are demanded from the coding system, the most simple BCD Code, i.e., 8-4-2-1, is decided upon as the best choice.

3.2.1 PARITY:-

It is well known that the B C D 8-4-2-1 is a non-error checking code but it can be made a single-error detecting code (either "even parity" or "odd parity") by adding a redundant bit to it in a suitable way. However, in the proposed counter type arithmetic, the coding does not play a very significant role and obviously the pay-off in terms of increased reliability will be so little that the considerable enhancement in cost to introduce parity (due to increased bit capacity in registers, counters, etc. and parity

checking procedure) can hardly be justified. So, the idea of obtaining parity has not been entertained in the present work although it can be introduced by the hardware designer afterwards, if found desirable.

3.3 THOUGHTS ON INPUT:-

Inputs to the desk calculator will be fed by pressing the appropriate keys on the console (numerals for data, i.e., numbers corresponding to operands, and others for commands) in the proper sequence (listed under Section 2.4) and for each pressing of a key, a standard pulse is needed in that line to be used for the machine operation. This can be achieved simply by using a micro-switch in series with a standard pulse generator; but the use of so many pulse generators will give rise to increased expense, non-identical pulses and decreased reliability. Instead, a better method will be to use a central pulse generator for all the keys and two simultaneously closing switches (normally both open) per each key. The scheme has been illustrated in the following diagram (Fig. 3.1).

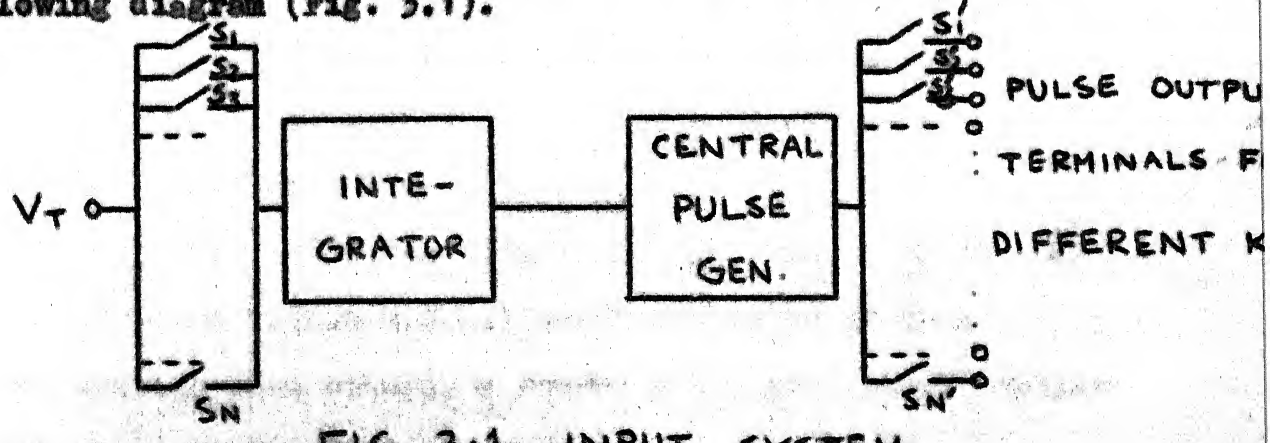


FIG. 3·1 INPUT SYSTEM

(i) In Fig. 3.1 V_T is the d.c. voltage from which the actuating voltage level of the pulse generator will be derived.

(ii) Pairs of switches (S_1 and S_1') or (S_2 and S_2') are normally open and close simultaneously by a single key-pressing; they should open out as soon as the key is released.

(iii) It is difficult to generate a single pulse from a switch or a relay closure because contacts bounce many times before making a solid contact. If these are connected directly to a pulse generator, they will produce a pulse for each contact bounce. To avoid that, an integrating circuit is connected between the contact and the pulse generator; this circuit converts the many fast voltage changes into a single slow change that generates a single pulse.

(iv) Since the actuating level is derived almost immediately on closing S_1 (or S_2, etc.) and S_1 & S_1', (or S_2 & S_2') remain closed so long as the key is kept pressed (say, for a few tenths of a second), the pulse will be transmitted faithfully through S_1' (or S_2' etc.) provided the order of delay between the closures of S_1 (or S_2 etc.) and S_1' (or S_2' etc.) is less than a millisecond. Otherwise, some delay will have to be introduced before each member of the second set of switches (i.e., S_1' , S_2', etc.).

(v) For the three "CLEAR" pulses (viz., "CLEAR ALL", "CLEAR S.R." and "CLEAR M.S.R.) which should be of much larger duration than others, a second pulse generator, similar to that shown in Fig. 3.1, is used.

3.3.1 METHOD OF ENTERING THE NUMBERS INTO EITHER OF THE TWO REGISTERS - S.R. AND M.S.R.:-

Since we have decided upon 8-4-2-1 B C D Coding (Section 3.2), each decimal digit, before being entered into S.R. (or M.S.R.), has to be encoded, into B C D 8-4-2-1 code. After encoding, appropriate logic is adopted to channelize the digit properly (i.e., either to S.R. or to M.S.R.). Fig. 3.2 illustrates the proposed method of number entry in block diagrams.

The following points should be noted in Fig. 3.2.

(i) S.R. and M.S.R. have not been drawn completely and nor have the interconnections and logic arrangement between the flip-flops been shown. Only 5 flip-flops in each register, corresponding to five bits at the extreme right, have been depicted for the purpose of illustration.

(ii) Diode-Capacitor-Diode (D-C-D) gating has been employed for triggering the flip-flops.

(iii) The levels L_S and L_M are complementary and for S.R. to take in the entry, L_S should be at "zero" level (L_M being at "one" level, disables M.S.R. to accept the entry). Similarly when L_S is at "one" level, M.S.R. (and not S.R.) will take in the digit.

3.4 DISPLAY SYSTEM:-

Although there are several standard methods of

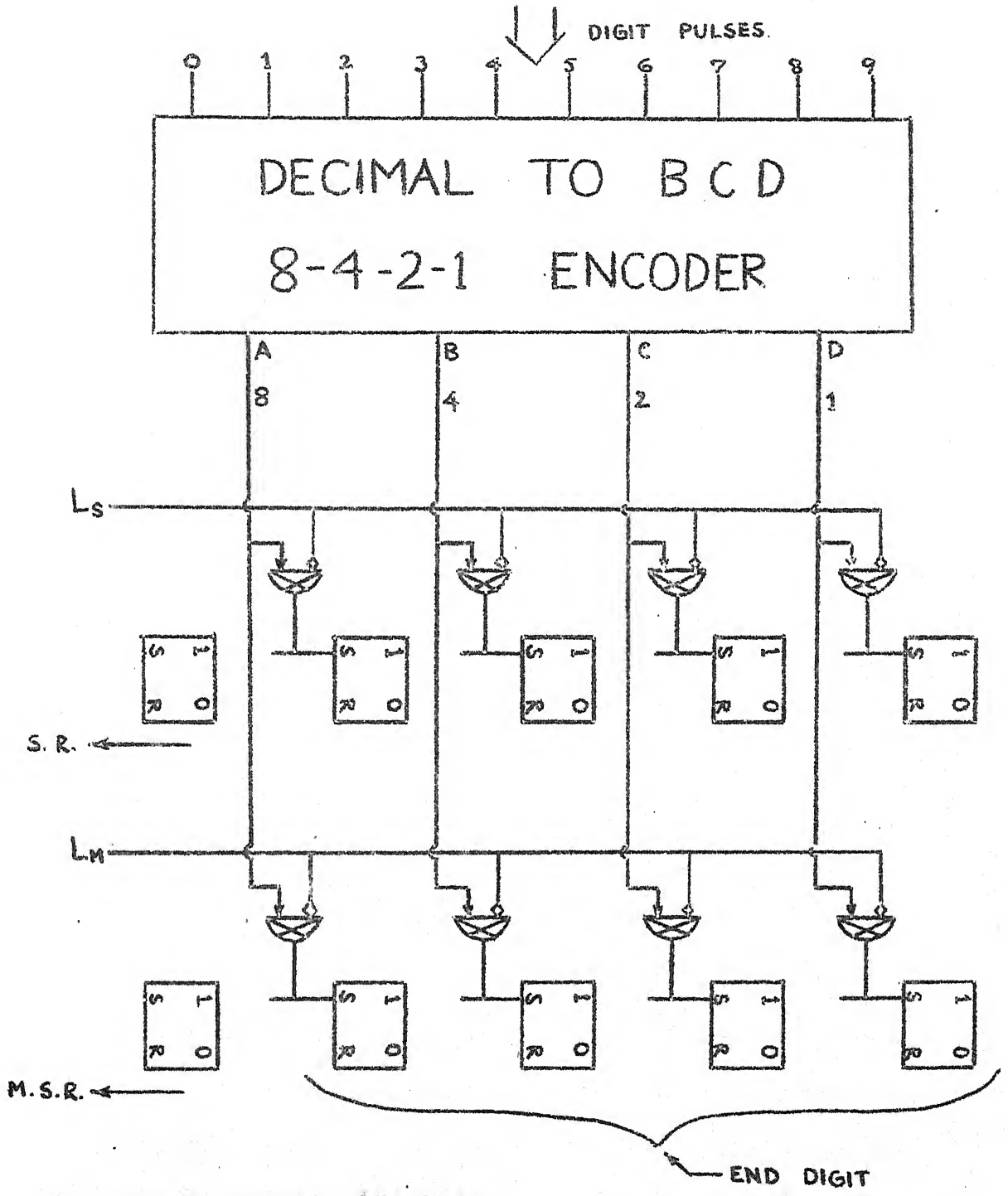


FIG. 3.2

DATA ENTRY INTO S. R. AND M. S. R.

obtaining in-line display while one or two indigenous and less expensive displays can be developed afterwards, for the present small machine it was decided to use NIXIE indicator tube display as a few of them are in stock.

NIXIE indicator tubes, available in either numeric or alpha-numeric configurations, are all electronic, gas-filled cold cathode display devices. The numeric tubes (which are going to be used with the present machine) consist of a common anode and ten individual metallic cathodes which are formed in the shape of numerals (0-9).

The device operates on the principle of the simple gas discharge diode. Application of a negative voltage to the selected cathode element with respect to the common anode causes the gas around the element to ionize and glow and only the selected character is visible in the common viewing area.

For operating the NIXIE tubes, transistor driver circuits have become the most popular method because of the availability of low cost high breakdown npn transistors. TRIXIE driver technique, which uses pre-biasing, has made possible the use of transistors with a breakdown voltage about 40% (around 65 volts) of the sustaining voltage (about 170 volts); the ON transistor is operated in a saturated condition and the OFF transistors in a back-biased condition.

Fig. 3.3 shows the operating circuit arrangement for a NIXIE tube, i.e., a NIXIE tube with its TRIXIE driver and blanking arrangement (blanking will be discussed in the next

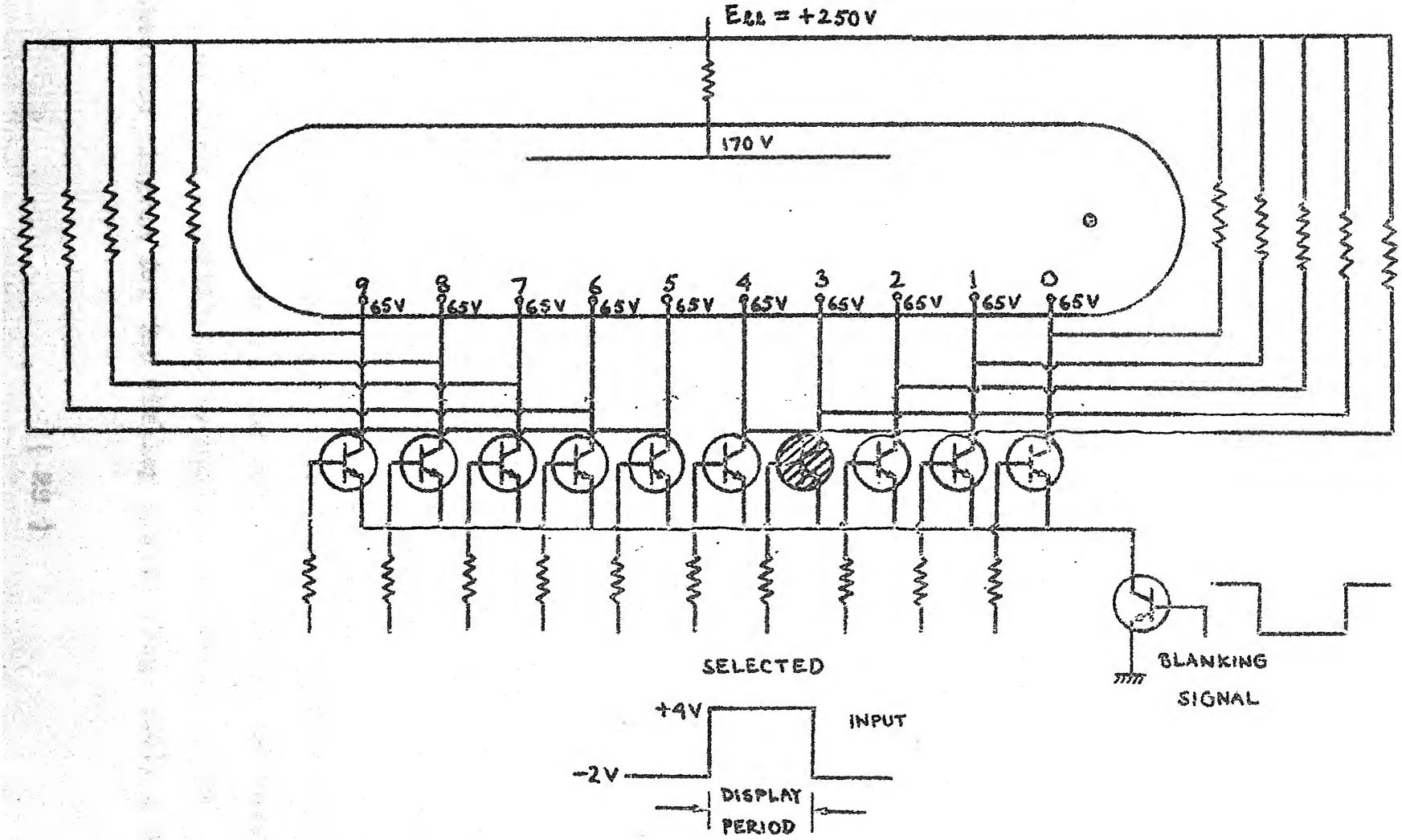


FIG. 3.3 A NIXIE TUBE WITH ASSOCIATED CIRCUITRY.

section, i.e., 3.4.1).

In Fig. 3.3, it should be noted that (i) the TRIXIE drivers need n p n transistors with a high breaddown voltage rating (more than 70 volts) and (ii) the voltages indicated at different points are just arbitrary.

3.4.1. BLANKING:-

Since in the present readout application, the rate of change of information to be displayed (system clock frequency is of the order of 50 Kc/s) will be faster than what the NIXIE tubes can possibly stand (minimum ionisation time is of the order of a few tenths of a millisecond), it will be desirable to have the NIXIE tubes lighted (ionized) only when data is to be observed. At all other times the display should be darkened even though the peripheral circuitry may still be accumulating data.

Blanking can be accomplished most simply by merely inserting a mechanical switch in the anode circuit of the tube. When the switch is closed, the full supply voltage is applied to the NIXIE tube anode. Assuming that input information is present on one of the cathodes of the tube, the corresponding data will be displayed.

Electronic methods of blanking are also achieved readily. But it is beyond the scope of the present work to discuss about a particular technique. However, in the schematic diagram for the display system (Fig. 3.4), a Set-Reset

flip-flop which can be used for controlling the voltage levels needed for blanking, has been included.

Fig. 3.4 illustrates the method of interconnections of different blocks for the display of a single digit (out of a total of five) in any of the three registers, viz., S.R., P.R. and M.S.R. In the diagram

(i) the technique of realising the blanking has not been indicated. However, a convention is adopted that the BLANKING FLIP-FLOP should be set for blanking.

(ii) for the display of the other four digits, connections should be extended to the other four NIXIE tubes from the appropriate points of the three registers and controlling flip-flops.

(iii) the relays shown in the diagram are of S P D T normally closed type.

3.4.2. DISPLAY CHART FOR THE OPERATOR:-

KEY PRESSED	DISPLAY UNIT CONNECTED TO	DISPLAY	GLOWING INDICATING LAMP
COMMON FOR ALL			
POWER ON	.....	Dark	*POWER ON INDICATING LAMP
CLEAR ALL	S.R.	Dark	
A. ADDITION/SUBTRACTION			
Ex 1. 2953 ± 72			
1. INDEX 2953			
(a) INDEX 2	S.R.	+ 00002	
(b) INDEX 9	S.R.	+ 00029	
(c) INDEX 4 (Wrong entry)	S.R.	+ 00294	
(d) CLEAR S.R.	S.R.	+ 00000	
(e) INDEX 2953	S.R.	+ 02953	
2. PRESS "+"	P.R.	+ 02953	
3. INDEX 72	S.R.	+ 00072	
4. PRESS "+" (or "-")	P.R.	+ 03025 (or + 02881)	
Ex 2. 72 - 2953			
4. PRESS "-"	P.R.	+ 97119	AMBER LAMP
5. PRESS "RESTORE"	P.R.	- 02881	
B. MULTIPLICATION			
Ex. 25 x 221			
2. PRESS "x"	S.R.	+ 00025	
3. INDEX 221	M.S.R.	+ 00221	
4. PRESS "="	P.R.	+ 05525	
C. DIVISION			
Ex. 8295 ÷ 23			
2. PRESS "÷"	P.R.	+ 08295	
3. INDEX 23	S.R.	+ 00023	
4. PRESS "÷"	M.S.R.	+ 00360	
5. PRESS "REMAINDER"	P.R.	+ 00015	

* POWER ON INDICATING LAMP remains ON throughout the entire period of operation of the Calculator.

CHAPTER - IV

4.1 ABOUT DIFFERENT REGISTERS AND COUNTERS TO BE USED:-

A brief description of the configuration and functions as well as the block diagram representation of the various registers and counters proposed to be used for achieving the operations of addition, subtraction, multiplication and division, is provided in this section.

(1) SETTING REGISTER (S.R.):

S.R. is a 5-digit capacity ring type (i.e., the tail feeds back to the mouth) shift register in which the numbers-inputs to the desk calculator can be entered. It is provided with the facility of reading-in the content of P.R. In the logic block diagrams, the S.R. will be represented as shown in Fig. 4.1(a).

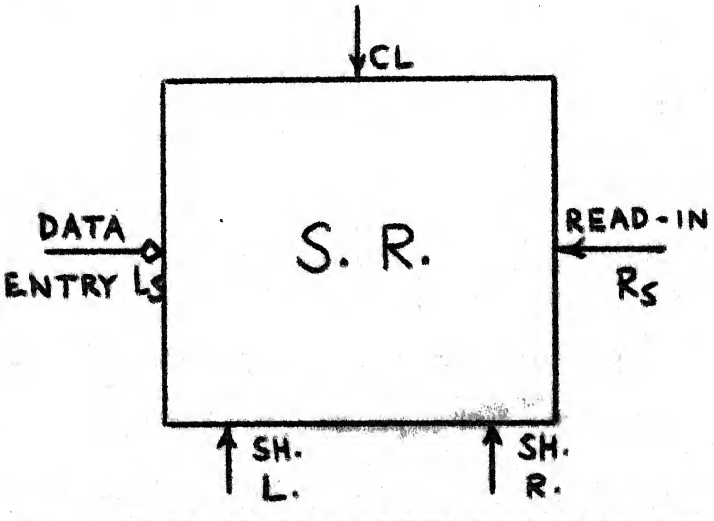


FIG. 4.1(a) BLOCK DIAGRAM REPRESENTATION OF S.R.

(2) PRODUCT REGISTER (P.R.):

This is a 5-digit UP-DOWN SHIFTABLE CASCADED DECADE COUNTER having individual input gates provided for the five decade counters, so that a digit (in fact, the corresponding number of pulses) can be entered at any one of the ones, tens, hundreds, thousands and ten thousands place. The actual place of entry of the digit is determined from the reading of the COUNTER-2 (described afterwards). P.R. is provided with reading-in facility. Fig. 4.1(b) shows the block diagram representation of P.R.

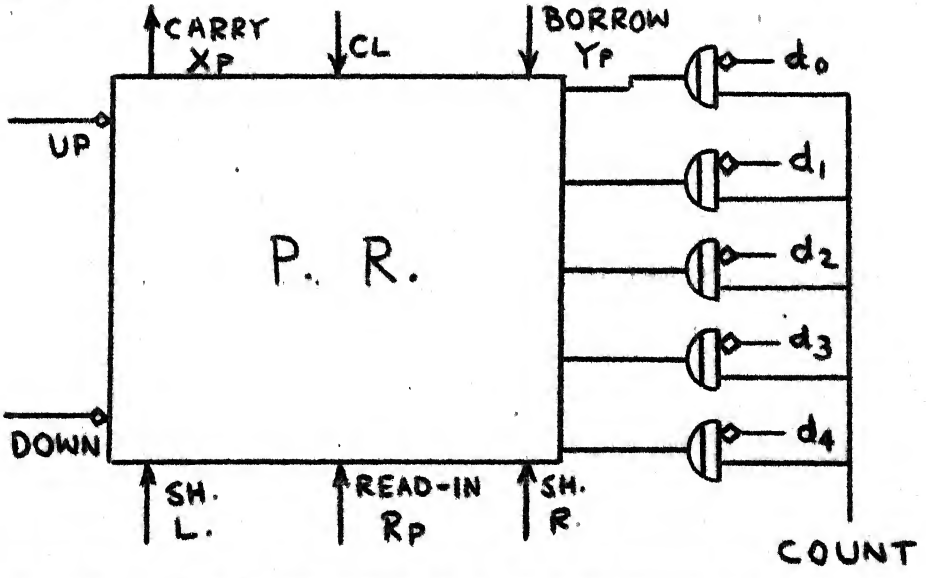


FIG. 4.1(b) BLOCK DIAGRAM REPRESENTATION OF P.R.

Note: d_0, d_1, d_2, d_3 and d_4 are the output levels of the diode matrix which decodes the reading of the COUNTER-2. For example, when COUNTER-2 reads 0 0 1 1 (i.e., 3) only d_3 will be "one" so that digit entry in P.R. will be at thousands place.

(3) MULTIPLIER SETTING REGISTER (M.S.R.):

M.S.R. is a 5-digit RING TYPE SHIFT REGISTER-CUM-CASCADED UP DECADE COUNTER in which the number-inputs to the desk calculator can be entered. It is also provided with reading-in facility and its block diagram representation is shown in Fig. 4.1(c).

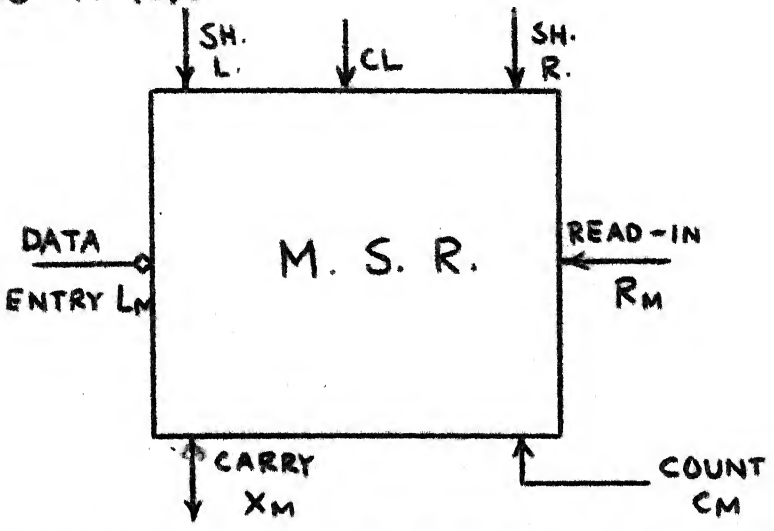


FIG. 4.1(c). BLOCK DIAGRAM REPRESENTATION OF M.S.R.

(4) COUNTER 1:

It is a DECADE DOWN COUNTER which can read-in the least significant digit in S.R. COUNTER 1 is represented in block diagram in Fig. 4.1(d).

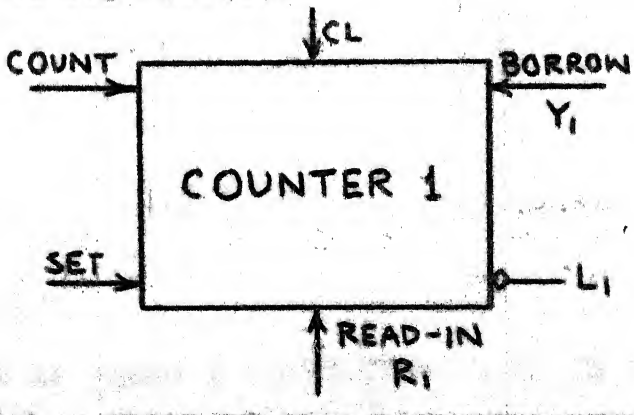


FIG. 4.1(d). BLOCK DIAGRAM REPRESENTATION OF COUNTER 1.

(5) COUNTER 2:

It is a COUNT-OF-FIVE UP COUNTER and its reading determines the place of entry of pulses corresponding to a digit into the P.R.

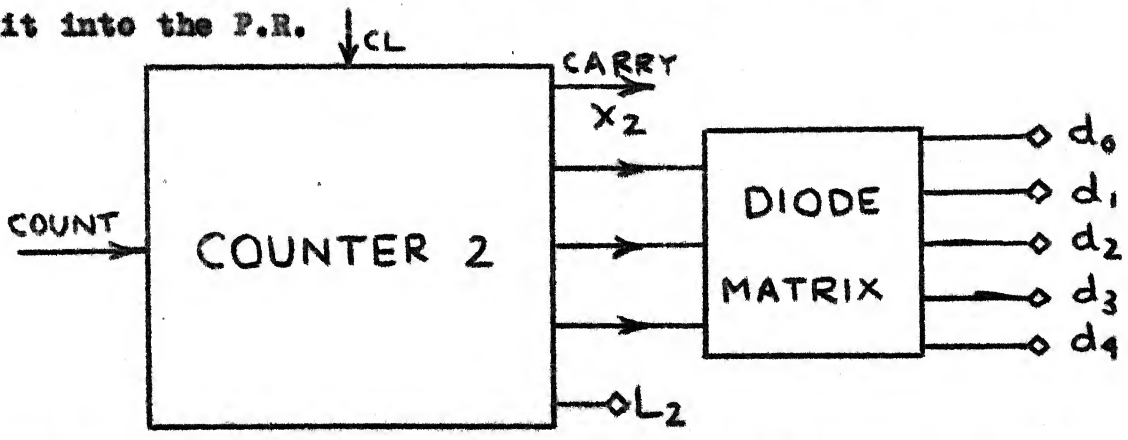


FIG. 4.1(e) BLOCK DIAGRAM REPRESENTATION OF COUNTER 2.

(6) COUNTER 3:

COUNTER 3, like COUNTER 1, is a DECADE DOWN COUNTER which can read-in the least significant digit in the M.S.R. [Fig. 4.1.(f)] .

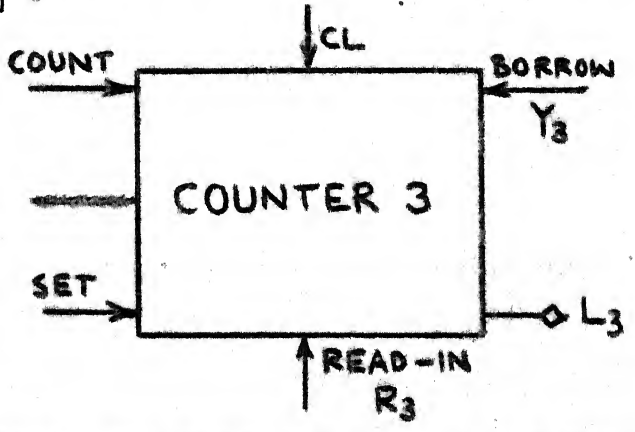


FIG. 4.1(f) BLOCK DIAGRAM REPRESENTATION OF COUNTER 3.

(7) COUNTER 4:

This is again a COUNT-OF-FIVE UP COUNTER.

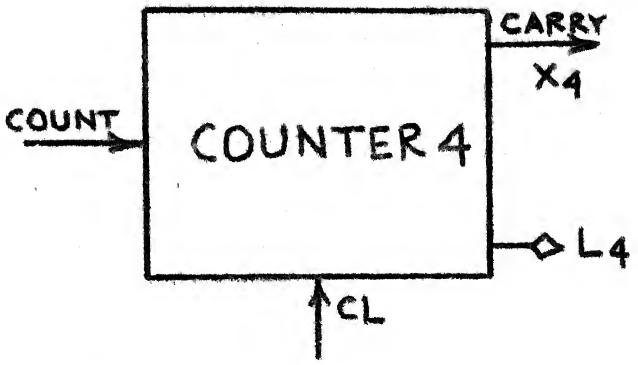


FIG. 4.1(g) BLOCK DIAGRAM REPRESENTATION OF COUNTER 4.

(8) DIGITS COUNTER:

It is a COUNT-OF-6 UP-DOWN COUNTER required only for the purpose of "digit-equalling" the two operands during division (Ref. Section 4.2.4).

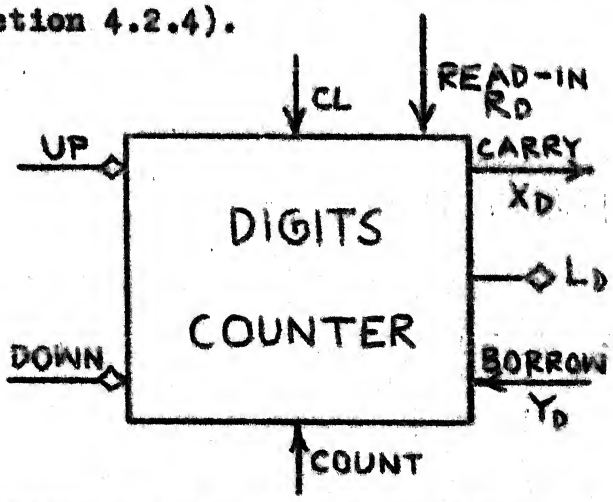


FIG. 4.1(h) BLOCK DIAGRAM REPRESENTATION OF DIGITS COUNTER.

Note: (i) In all the five counters, the levels L_1, L_2, L_3, L_4 & L_D are the level outputs of OR gates coupled to the five counters to sense when the corresponding counter reads 0. Obviously, L_1 (or L_2, ...) is 'zero' only when COUNTER 1 (or COUNTER 2, or .....) reads 0 and is 'one' otherwise.

(ii) Besides the five counters just described, a need for using one or two more counters may arise later on and consequently will be described at the appropriate point.

4.2 PRINCIPLE OF MACHINE ARITHMETIC:-

The counter type of arithmetic, i.e., the principle of achieving the mechanisation of the four basic arithmetical operations by adding, subtracting, repeatedly adding and repeatedly subtracting respectively number of pulses corresponding to the two operands, in UP-DOWN counters, is extremely straightforward and hardly needs any explanation. But if this principle is applied in a really "straightforward" way (for example, to multiply 220 by 95, 220 pulses are counted up 95 times, so that the total number of pulses entered into the counter is 20900 pulses), the operations will be fantastically slow and a multiplication of two 5-digit numbers may take as long as a few hours, even with a fairly high pulse repetition frequency! Consequently, this principle will have to be followed in conjunction with judicious application of shifting and other useful techniques. A detailed account of this modified principle is being provided below.

4.2.1 ADDITION:-

Ex. 72 + 2531 = 2603

In the process of addition (Ref. Section 2.4) the two important points that need explanation are

(A) How the numbers 72 or 2531 (i.e., the operands) are added from S.R. into P.R., and

(B) How the addend (i.e., 2531) is added to the augend (i.e., 72), already stored in P.R., i.e., how the addition takes place in P.R.

An attempt at providing sufficient explanations for the two points cited above is made as follows:

(A) Let the case of the augend (i.e., 72) be considered. The S.R. reads 00072 and P.R. reads 00000, M.S.R. not coming into picture at all. Also, both COUNTER 1 as well as COUNTER 2 read 0. Now,

(i) COUNTER 1 reads-in 2 (the least significant, i.e., the extreme right digit) from S.R. and is counted down by entering clock pulses. The same pulses which count down COUNTER 1 are entered into the ones place in P.R. (because COUNTER 2 reads 0 so that d_0 in Fig. 4.1(e) is 'one' and the 1's position input in P.R. is enabled) to count it up. So, on the completion of the counting down, P.R. reads 00002.

(ii) Now the S.R. is shifted right by one place so that it reads 20007 ('2' comes from the least significant to the most significant position because S.R. is a ring type shift register, as has been mentioned in Section 4.1) and a pulse is entered into COUNTER 2 to make it read 1. Thus "d_1" in Fig. 4.1(e) becomes 'one' and enables the 10's position input in P.R., so that on the next occasion, pulses to be entered into P.R. are entered in 10's position.

(iii) The steps (i) and (ii) are now repeated for the second least significant digit (i.e., 7) and at the end, P.R. reads 00072. The same procedure is continued for the other 3 digits in S.R. (incidentally all of them are zeros) and at the end of the operation of adding 72 from S.R. into P.R., the P.R. reads 00072 as desired.

S.R. is now cleared and the second operand, viz., 2531, is entered into S.R.

(B) The P.R. reads 00072 and the S.R. has stored 02531. Now, following the same procedures as explained in (A), all the five digits in S.R. are added into P.R., starting from 1 (the least significant digit). Probably it may be enough, for the purpose of explaining how the addition takes place in P.R., to tabulate the P.R. readings at the end of entry of each digit.

AFTER THE DIGIT X IS ADDED	P.R. READING
X = 1 (least significant)	0 0 0 7 3
X = 3 (2nd least significant)	0 0 1 0 3
X = 5 (3rd least significant)	0 0 6 0 3
X = 2 (4th least significant)	0 2 6 0 3
X = 0 (5th least significant)	0 2 6 0 3

Thus at the end of the operation, P.R. stores the desired sum 02603.

At this point one may possibly ask the question- for the first operand, instead of going through the addition cycle, why not jam transfer it directly from S.R. to P.R.? Thoughts have been given to this point and in the light of the following observations, the idea of jam transferring was set aside for effecting economy and simplicity in design.

(i) The apparent advantage of jam transfer is that it is extremely faster (needs only a few microseconds) compared to an addition cycle (takes a couple of milliseconds). However, in desk calculators, where the time interval between the depression of two keys is of the order of a second, this is obviously no consideration at all.

(ii) For the purpose of jam transferring the first operand and adding the second operand, the need for extra control logic arises, whereas this can be obviated by using the same addition cycle for the two operands; also in the former case extra gating is needed for achieving jam transfer.

4.2.2 SUBTRACTION:-

This is exactly the same process as ADDITION, the only difference being that the P.R. counts down when the subtrahend is entered into it from S.R.

4.2.3. MULTIPLICATION:-

Ex. 25 x 221 =

The operation of multiplication is mechanised by

repeated addition coupled with shifting at the appropriate points. According to the chosen example, S.R. and M.S.R. should store 00025 and 00221 respectively and it is noted that

$$25 \times 221 = 25 \times 1 + 250 \times 2 + 2500 \times 2$$

so that the procedure for performing multiplication will be

(i) The least significant digit (more appropriately the extreme right digit) in M.S.R., i.e.1, is read into COUNTER 3 and the content of S.R. is added into P.R. (by the same technique as was explained in Section 4.2.1) as many times, so that at the end P.R. reads 00025.

(ii) M.S.R. is shifted one place to the right to read 10022 (M.S.R. is also, like S.R., a ring type shift register) and S.R. is shifted one place to the left to read 00250.

(iii) Steps (i) and (ii) are repeated for the second time at the end of which P.R. reads 00525 [00025 + (00250 + 00250)] Also S.R. and M.S.R. reads 02500 and 21002 respectively.

(iv) Steps (i) and (ii) are repeated for another three times and the readings of the three registers are shown below at the end of each repetition

AFTER REPETITION FOR THE	S.R.	M.S.R.	P.R.
third time	25000	22100	05525
fourth time	50002	02210	05525
fifth time	00025	00221	05525

Thus when the process is terminated after repetition for the fifth time, P.R. stores the product 05525.

NOTE:

After the repetition for the fourth time the content of S.R. becomes 50002 instead of 250000 as expected, the reason for this distortion being the limited capacity of the S.R. However, this cannot introduce any error in the process of multiplication as this distorted content of S.R. is not added to the content of P.R. at all (because the corresponding least significant digit in M.S.R. has to be 0, provided the desired product is not to exceed 5 digits).

4.2.4 DIVISION:-

Ex. 8295 ÷ 23

The process of division is carried out by repeated subtraction coupled with shifting at the appropriate points. However, right at the outset, one very common but important question arises- what will happen if division by zero is attempted? Probably the best solution will be not to carry out the process of division at all in such a case and to signal the operator accordingly; consequently the present discussion of the principle of machine arithmetic for the process of division will incorporate this step.

According to the contents of Section 2.4 and with the chosen example, S.R. stores 00023 while P.R. has stored 08295, before the process of division starts. Now the

procedure for achieving the division will be:

(i) It is checked whether the divisor, stored in S.R., is zero. If it is zero then the process of division is not carried out at all and an indication is given to the operator to this regard, preferably by lighting the overflow indicating red lamp.

(ii) If in step (i) the divisor is found to be non-zero then with the help of the DIGITS COUNTER (which reads 2), the two operands are digit equalled (i.e., the number of digits in the divisor is made equal to that in the dividend) by shifting S.R. left by two places so that the readings of the three registers become

S.R. - 0 2 3 0 0 ; P.R. - 0 8 2 9 5 ; M.S.R. - 0 0 0 0 0 ;

However, before the start of the shifting process, the DIGITS Counter reading (i.e., 2) is jam transferred into a COUNT-OF-FIVE DOWN COUNTER, named CHECK COUNTER.

(iii) The content of S.R. is now subtracted repeatedly from that of P.R. and for each subtraction a pulse is entered into M.S.R. which is counting up. For the purpose of providing a clear and concise explanation of the whole procedure for achieving division, it will probably be worthwhile to keep track of the readings of the three registers after each subtraction as well as to describe the steps to be followed in succession, in the way shown below.

		M.S.R. READING	CHECK COUNTER READING
P.R. :	08295	00000	2
S.R. :	-02300		
	05995	00001	2
	-02300		
	03695	00002	2
	-02300		
	01395	00003	2
	-02300		
	↓ 99095	00003	2

Since with the last subtraction a borrow is obtained, no pulse is entered into the M.S.R. and instead the content of S.R. is added once to the content of P.R., i.e.,

		M.S.R. READING	CHECK COUNTER READING
P.R. :	99095	00003	2
S.R. :	02300		
	+		
	↑ 01395	00003	2

At this stage the CHECK COUNTER reading is tested for zero. Since it was not zero, the S.R. is shifted right by one place, the M.S.R. is shifted left by one place, a pulse is entered into the CHECK COUNTER to count it down and the process of repeated subtraction is started again:

		M.S.R. READING	CHECK COUNTER READING
P.R. :	01395	00030	1
S.R. :	00230		
	01165	00031	1
	00230		
	00935	00032	1
	00230		
	00705	00033	1
	00230		
	00475	00034	1
	00230		
	00245	00035	1
	00230		
	00015	00036	1
	00230		
	↑99785	00036	1

Since a borrow is obtained with the last subtraction, no pulse is entered into M.S.R. and instead the content of S.R. is <u>added</u> once to the content of P.R., i.e.

		M.S.R. READING	CHECK COUNTER READING
P.R. :	99785	00036	1
S.R. :	00230		
	↑00015	00036	1

At this stage the CHECK COUNTER reading is tested for zero. Since it was not zero, the S.R. is shifted right by one place, M.S.R. is shifted left by one place, a pulse is entered into the CHECK COUNTER to count it down and the process of repeated subtraction is started again

		M.S.R. READING	CHECK COUNTER READING
P.R. :	0 0 0 1 5	0 0 3 6 0	0
S.R. :	− 0 0 0 2 3		
	↓ 9 9 9 9 2	0 0 3 6 0	0

Since a borrow is obtained, no pulse is entered into M.S.R. and instead the content of S.R. is added once to the content of P.R., i.e.

		M.S.R. READING	CHECK COUNTER READING
P.R. :	9 9 9 9 2	0 0 3 6 0	0
S.R. :	+ 0 0 0 2 3		
	↑ 0 0 0 1 5	0 0 3 6 0	0

At this stage the CHECK COUNTER reading is tested for zero. Since it was zero, the process of division is discontinued and is deemed to have been completed. The quotient 00360 has been stored in the M.S.R. while the remainder 00015 is retained in the P.R.

4.3 DETAILED METHOD OF ACHIEVING THE PROPOSED ARITHMETIC:-

In Section 2.4 sequence of indexing and corresponding machine functions for carrying out different operations were listed. A detailed account of the method of realising these functions, in the light of what has been described in the previous Section, will be explained presently.

4.3.1 ADDITION:-

Ex. 2953 + 72.

1. PRESS "CLEAR ALL"-

(i) All registers and counters in the machine are cleared and the various flip-flops are returned to the starting or initial state.

(ii) The display is connected to S.R. and is blanked.

(iii) S.R. is made ready to take in the number going to be entered next, (i.e., the first operand in any of the four operations) and consequently entry to M.S.R. is blocked.

2. INDEX 2953-

(i) The most significant digit, i.e., 2 is pressed

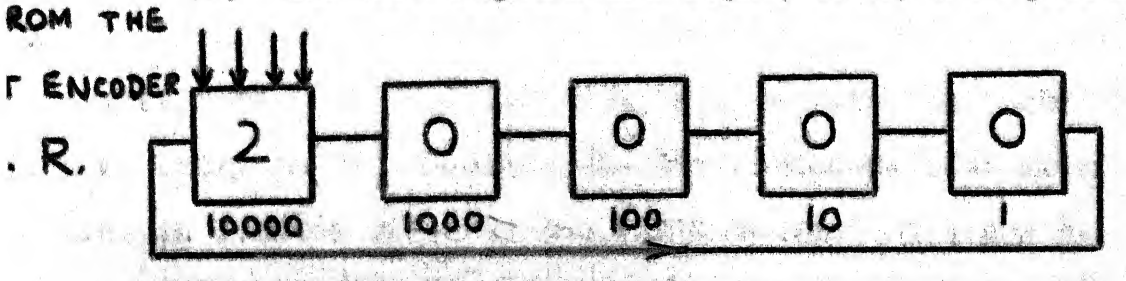


FIG. 4.2 ENTRY OF AN INDEXED NUMBER IN S.R.

and the digit 2 (in fact it is entered in BCD form, i.e., 0 0 1 0) is entered into S.R. in the 10000's position. The pulse corresponding to the digit blanks the display.

(ii) Automatically the S.R. (reading 2 0 0 0 0ø) is shifted one place to the left so that S.R. reads 00002 as desired. When the shifting is completed, the blanking on the display is withdrawn so that 00002 is read out by the operator.

(iii) Steps (i) and (ii) are repeated for the other 3 digits, viz., 9, 5 and 3 respectively. At the end of indexing the S.R. reads 02953 and is displayed.

At this stage, the other important readings are:
P.R. - 0 0 0 0 0 ; COUNTER 1 - 0 ; COUNTER 2 - 0.

5. PRESS "+" -

(i) The P.R. is set to count up.

(ii) The display is connected to P.R. and blanked.

(iii) COUNTER 1 reads-in the least significant (i.e., the extreme right) digit 3 from S.R. Clock pulses are entered into COUNTER 1 to count it down to zero and each pulse is also entered into P.R. (The place of entry in P.R., as determined from COUNTER 2 reading, is one's now since "d_0" is 'one').

(iv) The counting down in step (iii) stops when the COUNTER 1 reads zero. Then P.R. reads 00003 and (a) a pulse is entered into COUNTER 2 (so that "d_1" becomes "one" and the place of entry in P.R. becomes the ten's counter), as also (b) S.R. is shifted right by one digit to read 3 0 2 9 5.

(v) Steps (iii) and (iv) are now repeated for the

other four digits in S.R. (i.e., 5, 9, 2 and 0), starting from the second least significant digit (at present the extreme right digit), 5. At the end of this operation, the P.R. reads 0 2 9 5 3, S.R. reads 0 2 9 5 3 and COUNTER 2 reads 0 after giving out a carry (because it is a count-of-5 up counter).

Steps (iii) through (v) constitute an "ADDITION/ SUBTRACTION CYCLE".

(vi) The carry obtained from COUNTER 2 in step (v) indicates the end of the operation and (a) clears the S.R. and (b) removes the blanking of the NIXIE tubes so that the content of P.R. (i.e., 0 2 9 5 3) is displayed.

4. INDEX 72 - The sequence of functions is exactly same as explained in Step 2 (i.e., INDEX 2953). However, in addition

(iv) as soon as the first digit (i.e., most significant digit) 7 is entered, the display is connected back to S.R. from P.R.

5. PRESS "+" - The same sequence of functions as explained in 3 (PRESS "+") is repeated.

Thus at the end of the operation of ADDITION, the P.R., storing the sum 0 3 0 2 5 is displayed.

4.3.2 <u>SUBTRACTION</u>:-

CASE (i): Ex. 2531-72.

The sequence of indexing and the functions performed

by the machine are exactly similar to those in Section 4.3.1 (i.e., ADDITION), except that in 5, instead of PRESS "+", it will be PRESS "-" in this case. Correspondingly, there will be a change in step (i) under 5, viz.

(i) The P.R. is set to count down (instead of counting up).

CASE (ii) : Ex. 72-2953

This case is similar to CASE (i). However, at the end of the functions corresponding to 5 (i.e., PRESS "-"), the subtrahend being greater than the minuend, P.R. displays the negative difference in the complement form. This is also indicated by the glow of an amber lamp.

In order to get the result in the normal form, i.e., 02881, the "RESTORE" key is pressed.

6. PRESS "RESTORE" -

(i) P.R. is set to count down.

(ii) The display is blanked and the connection of the NIXIE tube displaying sign is shifted to the negative cathode.

(iii) S.R. reads-in the content of P.R.

(iv) P.R. is cleared.

(v) The content of S.R. is subtracted once from the content of P.R., at the end of which (a) the S.R. is cleared and (b) the blanking of the display is removed.

Thus finally P.R., containing 0 2 8 8 1 is displayed with a negative sign (the principle of restoration was explained in Section 2.4 B).

4.3.3 MULTIPLICATION:-

Ex. 25 x 221 =

1. PRESS "CLEAR ALL" - Already explained.

2. INDEX 25 - As in 2 in Section 4.3.1, 25 is entered into S.R., which reads 0 0 0 2 5.

3. PRESS "X" -

(i) M.S.R. is enabled to take in the next operand (i.e., multiplier), while the entry to S.R. is blocked.

(ii) The display is kept connected to S.R.

4. INDEX 221 - Besides performing the three functions listed in 2 in Section 4.3.1 (only difference being that the number 221 is entered into M.S.R. instead of S.R. which retains 00025), it does one more thing, viz.

(iv) As soon as the first digit, i.e., 2 is entered, the display is connected to M.S.R. from P.R.

5. PRESS "=" -

(i) The P.R. is set to count up.

(ii) The display is connected to P.R. and blanked.

(iii) COUNTER 3 is made to read-in the least significant digit (in fact the extreme right digit), i.e., 1 from M.S.R.

(iv) An ADDITION/SUBTRACTION CYCLE is initiated and at the end of the cycle, a pulse is entered into COUNTER 3 to count it down.

(v) If the COUNTER 3 reading now is not zero, (in the

present example it will be zero), step (iv) is continued till COUNTER 3 reads zero.

(vi) When COUNTER 3 reads zero, a pulse is entered into COUNTER 4 (which always counts up) and S.R. as well as M.S.R. are shifted one place to the left and right respectively.

(vii) Since COUNTER 4 reading is non-zero (in fact it is 1), the steps (iii) through (vi) are repeated and this continues till COUNTER 4 reads 0. (Four repetitions are actually needed for the COUNTER 4 to read zero as it is a count-of-five counter).

(viii) As soon as COUNTER 4 reads zero (simultaneously giving out a carry), the end of the multiplication process is indicated.

Note:- Steps (iii) through (viii) constitute a "MULTIPLICATION CYCLE".

(ix) The carry obtained from COUNTER 4 in step (viii) (a) clears the S.R. and M.S.R. and (b) removes the blanking on the NIXIE tubes so that the product stored in P.R. is displayed.

4.3.4 DIVISION:-

Ex. 8295 ÷ 23

1. PRESS "CLEAR ALL" - Over and above all the three functions formulated previously (Section 4.3.1), one more addition to the list is needed in case of division (because of the requirement of "digit equalling") viz., (iv) the DIGITS counter is enabled and set to count up.

Note:- Each digit pulse will always be input to the DIGITS counter, which may be enabled or disabled, counting up or down.

2. INDEX 8295 - Same as explained in 2 in Section 4.3.1. However, each digit pulse having been entered into the DIGITS counter, it reads 4 at the end, the S.R. reading being 0 8 2 9 5.

Note:- At this point, it will probably be appropriate to mention an important point about the exact way of entering data. Although 35 or 035 or 0035 or 00035 are the same mathematically, yet the number 35 should be entered only as 35 (by pressing first 3 and next 5) and not as 035 (or 0035, or 00035). This is essential for achieving a correct process of division, as should be clear from the stated use of the DIGITS counter.

3. PRESS "÷" -

(i) The P.R. is set to count up.

(ii) The DIGITS counter, still enabled, is set to count down.

(iii) The display is connected to P.R. and is blanked.

(iv) An ADDITION/SUBTRACTION CYCLE is initiated so that the content of S.R. is added once to that of P.R., giving out a carry from COUNTER 2 at the end of the operation.

(v) This carry is used to (a) clear S.R. and (b) remove the blanking on the display so that the dividend (i.e., 0 8 2 9 5) stored in P.R. is displayed.

4. INDEX 23 - 23 is entered into S.R. in the usual manner. Each digit pulse having been entered into the DIGITS COUNTER (counting down), it reads 2 now. Moreover, as in 4 in Section 4.3.1,

(iv) As soon as the first digit, i.e., 2 is entered, the display is connected back to S.R. from P.R.

Note:- If division of a smaller digit number by a larger digit number (it is not allowed in the present machine) is attempted, the DIGITS counter gives out a carry which, like "CLEAR ALL" pulse, clears the entire machine, blanks the display suddenly and lights the OVERFLOW INDICATING RED LAMP. All these should serve as enough indications to the operator to press the "CLEAR ALL" key and start the entire operation anew.

5. PRESS "$\div$" -

(i) It is checked whether the divisor, stored in S.R., is zero. (Since S.R. is still connected to the display unit, this divisor-checking can be easily done by AND ing the 'O' line outputs of the five B C D 8-4-2-1 TO DECIMAL DECODERS, one of which has been shown in Fig. 3.4). If the divisor is found to be zero, then the overflow indicating red lamp is lighted so that the operator immediately presses the CLEAR ALL key. If the divisor is found to be non-zero, then

(ii) The P.R. is set to count down.

(iii) The display is connected to M.S.R. and is blanked.

(iv) The DIGITS counter reading is tested for zero and since it is found to be non-zero, "digit-equalling" has to

be done. So, (a) the CHECK counter is made to read-in the content of the DIGITS counter and (b) S.R. is shifted to the left and one pulse per each shifting is entered into the DIGITS counter (counting down). The shifting is discontinued as soon as the DIGITS counter reading becomes zero. Thus, for digit equalling of the dividend and the divisor, two shiftings have been required; consequently the readings of the three registers have become

S.R. : 0 2 3 0 0 ; P.R. : 0 8 2 9 5 ; M.S.R. : 0 0 0

with DIGITS counter and CHECK counter readings being 0 and 2 respectively.

(v) The CHECK counter is enabled to count down.

Note:- If the DIGITS counter reading in the beginning of step (iv) were found to be zero, then the latter part of step (iv) as well as step (v) could be skipped.

(vi) Now an ADDITION/SUBTRACTION CYCLE is initiated so that the divisor (in S.R.) is subtracted once from the dividend (in P.R.). At the end of the cycle, a carry pulse is given out by COUNTER 2.

(vii) If there was obtained no borrow from the P.R. in step (vi), the carry pulse is entered into the M.S.R. to count it up and the step (vi) is repeated.

(viii) The cycle comprising of steps (vi) & (vii) is repeated so long as no borrow is obtained from P.R. in step (vi).

(ix) If a borrow is obtained from the P.R. at the end of step (vi), (a) no pulse is entered into the M.S.R.,

(b) the P.R. is set to count up and (c) an ADDITION/SUBTRACTION CYCLE is initiated so that the content of S.R. is added once to the content of P.R. At the end of (c), as usual a carry pulse is given out by COUNTER 2.

(x) When the carry pulse is obtained at the end of step (ix), (a) the P.R. is set to count down and (b) the reading of the CHECK counter is tested for zero.

(xi) If the CHECK counter reading in step (x) is not zero, (a) the S.R. is shifted right by one place, (b) the M.S.R. is shifted left by one place, (c) a pulse is entered into the CHECK counter (counting down) and (d) the steps (vi) through (x) are repeated.

(xii) If the CHECK counter reading in step (x) is a zero, the whole process of division is discontinued and deemed to have ended with the quotient and the remainder stored in the M.S.R. and the P.R. respectively.

Note:- Steps (vi) through (xii) constitute a "DIVISION CYCLE".

(xiii) The blanking of the display is now removed so that the M.S.R., storing the quotient, is displayed.

6. PRESS "REMAINDER" - The display is connected to the P.R. so that the remainder is displayed.

4.3.5 BEHAVIOUR OF THE DIGITS COUNTER DURING THE FOUR OPERATIONS AS WELL AS WITH THE PULSES "CLEAR S.R." AND "CLEAR M.S.R.":-

The mode of functioning of the DIGITS counter which is,

incidentally, useful only during the process of division, can be formulated, as described below, for the four operations of addition, multiplication, subtraction and division.

KEY PRESSED		BEHAVIOUR OF THE DIGITS COUNTER
"CLEAR ALL"	-	The DIGITS counter is reset, enabled and set to count up.
"NUMERALS" FOR THE FIRST OPERAND	-	A pulse per each digit is entered into the DIGITS counter (counting up).
"+" OR "-" OR "x"	-	The DIGITS counter is disabled and reset.
"÷"	-	The DIGITS counter, still enabled, is set to count down.
"NUMERALS" FOR THE SECOND OPERAND	-	A pulse per each digit is entered into the DIGITS counter (counting down) <u>only for the divisor</u> while digit pulses corresponding to the addend, subtrahend and multiplier, find the DIGITS counter disabled.
"="	-	The DIGITS counter remains unaffected.
"÷"	-	The DIGITS counter reading is tested for zero. If it is not a zero, S.R. is shifted left and one pulse per each shifting is entered into the DIGITS counter (counting down); the shifting is discontinued as soon as the DIGITS counter reads zero.

The above formulation, however, has not taken into consideration what will happen to the DIGITS counter reading in the event of the use of the two keys- "CLEAR S.R." and "CLEAR M.S.R.", which are used when operands are wrongly entered into the two registers. This problem has been investigated and a suitable solution has been proposed below.

A. ADDITION/SUBTRACTION:-

Ex. 2953 ± 72

(Let it be assumed that a mistake is committed in the third digit while entering the first operand, i.e., 2953).

ACTION	BEHAVICUR OF THE DIGITS COUNTER
"CLEAR ALL" key is pressed.	- The DIGITS COUNTER is cleared, enabled and set to count up.
The first operand is wrongly entered.	- The DIGITS counter reads 3.
"CLEAR S.R." key is pressed.	- The DIGITS counter is cleared.
The first operand is correctly entered.	- The DIGITS counter reads 4.
"+" key is pressed	- The DIGITS counter is reset and disabled.

The latter part of the computation need not be given any consideration as the DIGITS counter has been disabled.

B. MULTIPLICATION:-

Ex. 25 x 221

The behaviour of the DIGITS counter in this case will

be exactly similar to that for ADDITION/SUBTRACTION, only point that deserves a mention being that the DIGITS counter is not affected by the "CLEAR M.S.R." key as it was already disabled by the "x" key.

C. DIVISION:-

Ex. 8295 ÷ 23.

Behaviour of the DIGITS counter before the "÷" key is pressed has already been explained under ADDITION/SUBTRACTION, so that the "÷" key can be starting point for the present case.

ACTION		BEHAVIOUR OF THE DIGITS COUNTER
"÷" Key is pressed	-	The DIGITS counter, storing 4, is set to count down (it remains enabled).
The DIVISOR is wrongly entered (mistake in the second digit, say)	-	The DIGITS counter reads 2 (4-2).
"CLEAR S.R." key is pressed.	-	The DIGITS counter is reset to read zero. (So the number of digits in the dividend, i.e., 4, is lost!).

Thus the above action corresponding to the "CLEAR S.R." key, although works for ADDITION, SUBTRACTION and MULTIPLICATION, brings in trouble during DIVISION. However, it can be easily rectified by the use of an additional 3-bit register with jam transfer facility, the scheme being as illustrated below.

ACTION		BEHAVIOUR OF THE DIGITS COUNTER
"÷" key is pressed	-	The DIGITS counter, storing 4, is set to count down. Also the content of the DIGITS counter is jam transferred into the additional register called the CORRECTION REGISTER, which thus stores 4.
The divisor is wrongly entered.	-	The DIGITS counter reads 2 (4.2).
"CLEAR S.R." key is pressed-	-	The DIGITS counter is reset as usual but then it reads-in 4 from the CORRECTION REGISTER (which still stores 4 for possible use in case of a second wrong entry).
The divisor is correctly entered.	-	The DIGITS counter reads 2 (4.2).

Now the process of division can be carried out without any possibility of mistake.

4.4 OPERATIONS CORRESPONDING TO DIFFERENT KEYS:-

In this section the important functions to be performed by the different keys will be listed. This will be done to provide guidelines for the logical design, from what have been presented so far, and does not necessarily include each and every operation to be actually performed.

1. ON/OFF SWITCH:- Power supply for the entire machine is turned on or off.

2. "CLEAR ALL " -

(i) All registers and counters in the machine are cleared and the various flip-flops are returned to the starting or initial state.

(ii) The display is connected to S.R. and is blanked.

(iii) The S.R. is made ready to accept the next entry (i.e., the first operand for any of the four operations) and consequently entry into M.S.R. is blocked.

(iv) The DIGITS counter is enabled and set to count up.

3. "CLEAR S.R." -

(i) The S.R. as well as the DIGITS counter is cleared.

(ii) The content of the CORRECTION REGISTER is read into the DIGITS counter only during the entry of the divisor.

4. "CLEAR M.S.R." - Only M.S.R. is cleared.

5. NUMERALS -

(i) The pulse corresponding to each digit blanks the display.

(ii) As soon as a digit is entered, the S.R. or the M.S.R., as the case may be, is shifted left by one place and immediately after completion of the shifting, blanking on the display is withdrawn.

(iii) Each digit pulse is input to the DIGITS counter which may be enabled or disabled and counting up or down, depending on the different operations and the particular sequence

in the same operation.

(iv) With the first digit pulse of the second operand during any of the four operations, the display is connected either from P.R. to S.R. (for addition, subtraction and division) or from S.R. to M.S.R. (for multiplication).

6. "+" -

(i) The P.R. is set to count up.

(ii) The display is connected to P.R. and is blanked.

(iii) The DIGITS counter is disabled and reset.

(iv) An ADDITION/SUBTRACTION CYCLE is started to add the content of S.R. to the content of P.R. At the end of the cycle, a carry is generated from COUNTER 2.

(v) The carry obtained in step (iv) is used to (a) clear the S.R. and (b) remove the blanking of the display.

7. "-" - Same as that for "+", except that in step (i), the P.R. will be set to count <u>down</u>.

8. "x" -

(i) M.S.R. is enabled to accept the next operand (i.e., multiplier) while entry to S.R. is blocked.

(ii) The DIGITS counter is disabled and reset.

9. "÷" -

(i) The P.R. is set to count up.

(ii) The DIGITS counter, still enabled, is set to count down.

(iii) The display is connected to P.R. and is blanked.

(iv) An ADDITION/SUBTRACTION CYCLE is initiated so that the content of S.R. (i.e., the dividend) is added to that of P.R. (zero), giving out a carry from COUNTER 2 at the end of the operation.

(v) This carry in step (iv) (a) clears the S.R., (b) removes the blanking on the NIXIE tubes and (c) jam transfers the content of the DIGITS counter into the CORRECTION REGISTER.

10. "=" -

(i) The P.R. is set to count up.

(ii) The display is connected to P.R. and blanked.

(iii) A MULTIPLICATION CYCLE (see Section 4.3.3) is initiated, at the end of which a carry is given out by COUNTER 4.

(iv) The carry obtained as above (a) clears the S.R. and M.S.R. and (b) removes the blanking on the NIXIE tubes.

11. "÷" -

(i) It is checked whether the divisor, stored in S.R., is zero. If the divisor is found to be zero, then the overflow indicating red lamp is lighted. If the divisor is found to be non-zero, then

(ii) The P.R. is set to count down.

(iii) The display is connected to M.S.R. and is blanked.

(iv) The DIGITS counter reading is tested for zero. If it is zero, the machine directly goes to the next step. However, if it is found to be non-zero, then (a) the CHECK counter reads-in the content of the DIGITS counter; (b) S.R. is shifted

to the left and one pulse per each shifting is entered into the DIGITS counter (counting down). The shifting is discontinued as soon as the DIGITS counter reading becomes zero. (c) Also the CHECK counter is enabled to count down.

Steps iv(a) through iv(c) constitute "digit-equalling procedure".

(v) A DIVISION CYCLE (see Section 4.3.4) is initiated.

(vi) At the end of the DIVISION CYCLE, the blanking is withdrawn from the display.

12. "RESTORE" -

(i) The P.R. is set to count down.

(ii) The display is blanked.

(iii) The negative cathode of the NIXIE tube for displaying sign is connected in place of the positive cathode.

(iv) S.R. reads-in the content of P.R.

(v) P.R. is cleared.

(vi) An ADDITION/SUBTRACTION CYCLE is started to subtract the content of S.R. from that of P.R. and it gives out a carry from COUNTER 2 at the end.

(vii) The carry thus obtained (a) clears S.R. and (b) removes the blanking of the display.

13. "REMAINDER" - The display is connected to P.R.

4.4.1 <u>ABOUT THE INDICATING LAMPS</u>:-

As already listed in Section 2.5, there are three indicating lamps (neon) on the console and below is provided a

brief description of their uses and utilities.

1. COMPLEMENT FORM INDICATING AMBER LAMP:

This lamp glows whenever the content of P.R. is in a complement form and is useful during subtraction of a larger number from a smaller number, where the process of restoring (Section 2.4 B) is needed. During the process of division also this lamp will glow for a few times (whenever a borrow is obtained from P.R.) but only for an extremely short while unlike during subtraction when the glow is permanent. The lamp is extinguished as soon as the "RESTORE" key is pressed.

2. OVERFLOW INDICATING RED LAMP:

During the operations of ADDITION and MULTIPLICATION, the sum or the product may exceed the capacity of P.R. and an overflow may occur. The Overflow Indicating Red Lamp glows whenever this occurs and the operation should be stopped by pressing the CLEAR ALL key which makes the red lamp go off.

The Overflow Indicating Red Lamp also glows when a (i) division by zero (O) or (ii) division of a smaller number by a larger number is attempted and will be extinguished as soon as the CLEAR ALL key is pressed.

3. 'POWER ON' INDICATING LAMP:

This lamp is ON so long as the machine is supplied with power and it remains extinguished so long as the Power Supply is OFF.

4.5 DETAILED LOGICAL DESIGN AND DIAGRAMS:-

Based on the materials presented so far, especially in Sections 4.3 and 4.4, detailed logical design has been carried out in the present Section for the independent operations of 1. SHIFT PULSE GENERATION, 2. ENTERING NUMBERS INTO S.R. OR M.S.R., 3. ADDITION/SUBTRACTION, 4. MULTIPLICATION, and 5. DIVISION, to be performed by the machine. The symbols and representations of different logical blocks and quantities have been listed partly in Section 4.1 and partly in APPENDIX A; however, the notations used for the various pulses, levels, etc. in the logic diagrams have been explained along with the relevant diagrams. Care has been taken to see that

(i) Left and right shifting pulses do not enter any register simultaneously.

(ii) Both the counting up level as well as the counting down level are not enabled simultaneously in an UP-DOWN counter.

(iii) Only one register is connected to the display unit at a time.

(iv) Half pulses are not entered into counters and shift registers.

4.5.1 SHIFT PULSE GENERATION:-

In order to shift a register one place (i.e., by a digit), a set of four shift pulses are required (because a decimal digit is represented by four bits) and consequently the

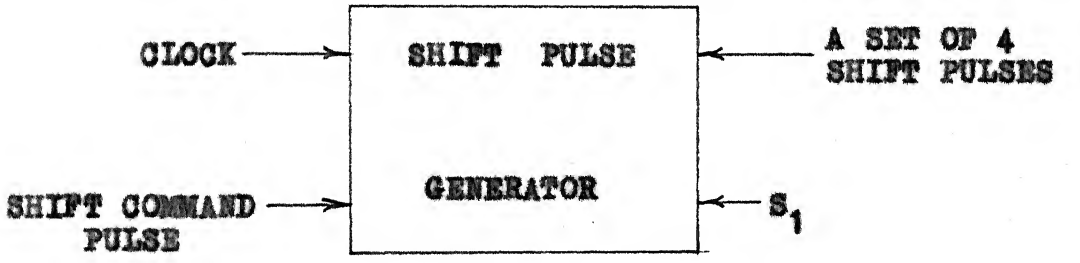
SHIFT PULSE GENERATOR should deliver a set of four shift pulses followed by an extra pulse to indicate the completion of the set (this is extremely important as well as useful), after the command pulse is fed into it. Fig. 4.2 is a block logic diagram of the SHIFT PULSE GENERATOR.

In Fig. 4.2

(i) S_1 is the pulse given out after the completion of the set of shift pulses.

(ii) Some of the logic blocks have been numbered for future reference.

The block diagram representation of the SHIFT PULSE GENERATOR for future use will be as shown below:



4.5.2 ENTERING NUMBERS INTO S.R. OR M.S.R.:-

Fig. 4.3 shows a logical arrangement designed for the purpose of entering numbers into either S.R. or M.S.R. as the requirement may be. The various notations used in the diagram are explained below.

P_A Pulse corresponding to "CLEAR ALL" key.

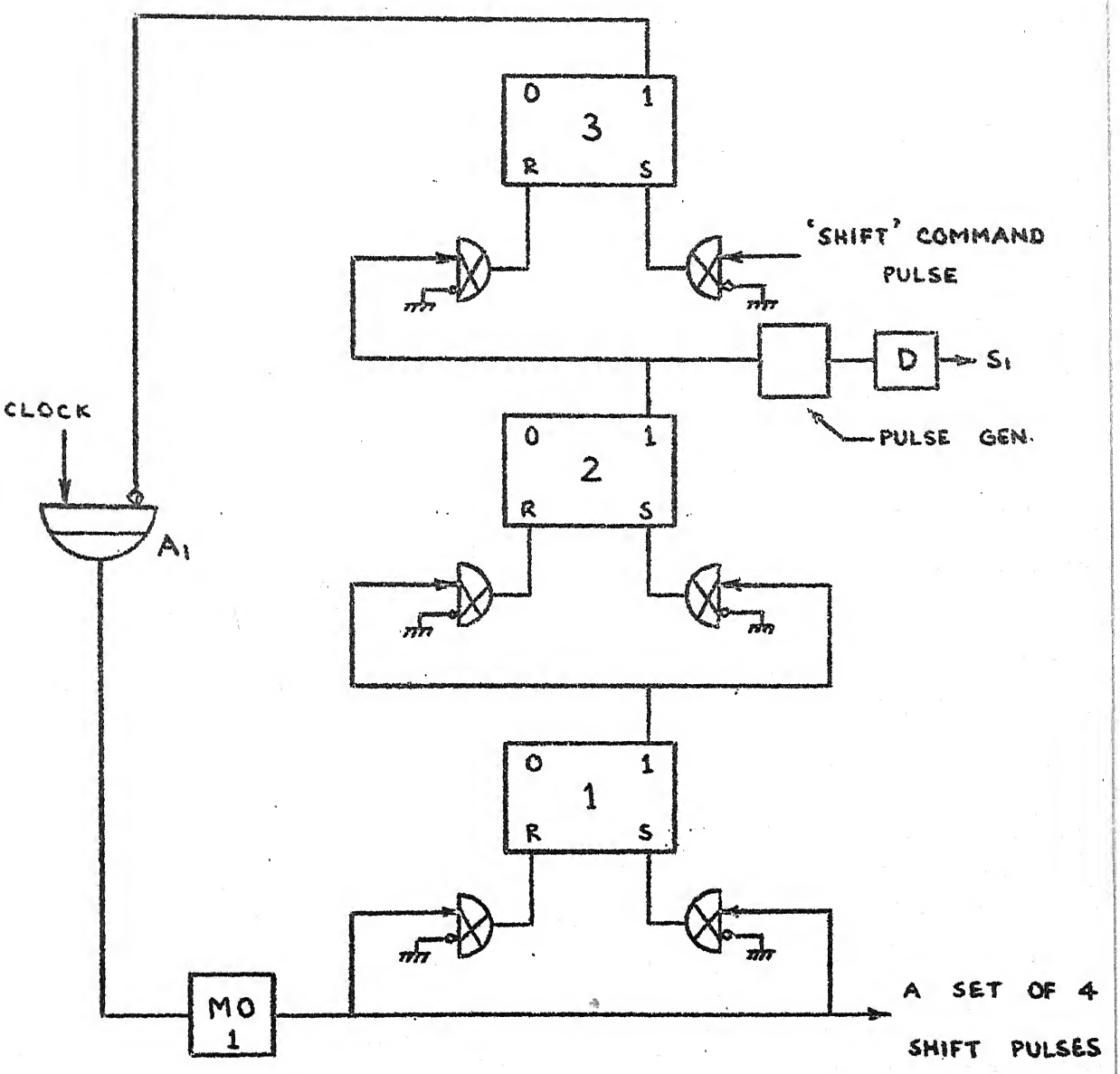


FIG. 4·2

SHIFT PULSE GENERATOR

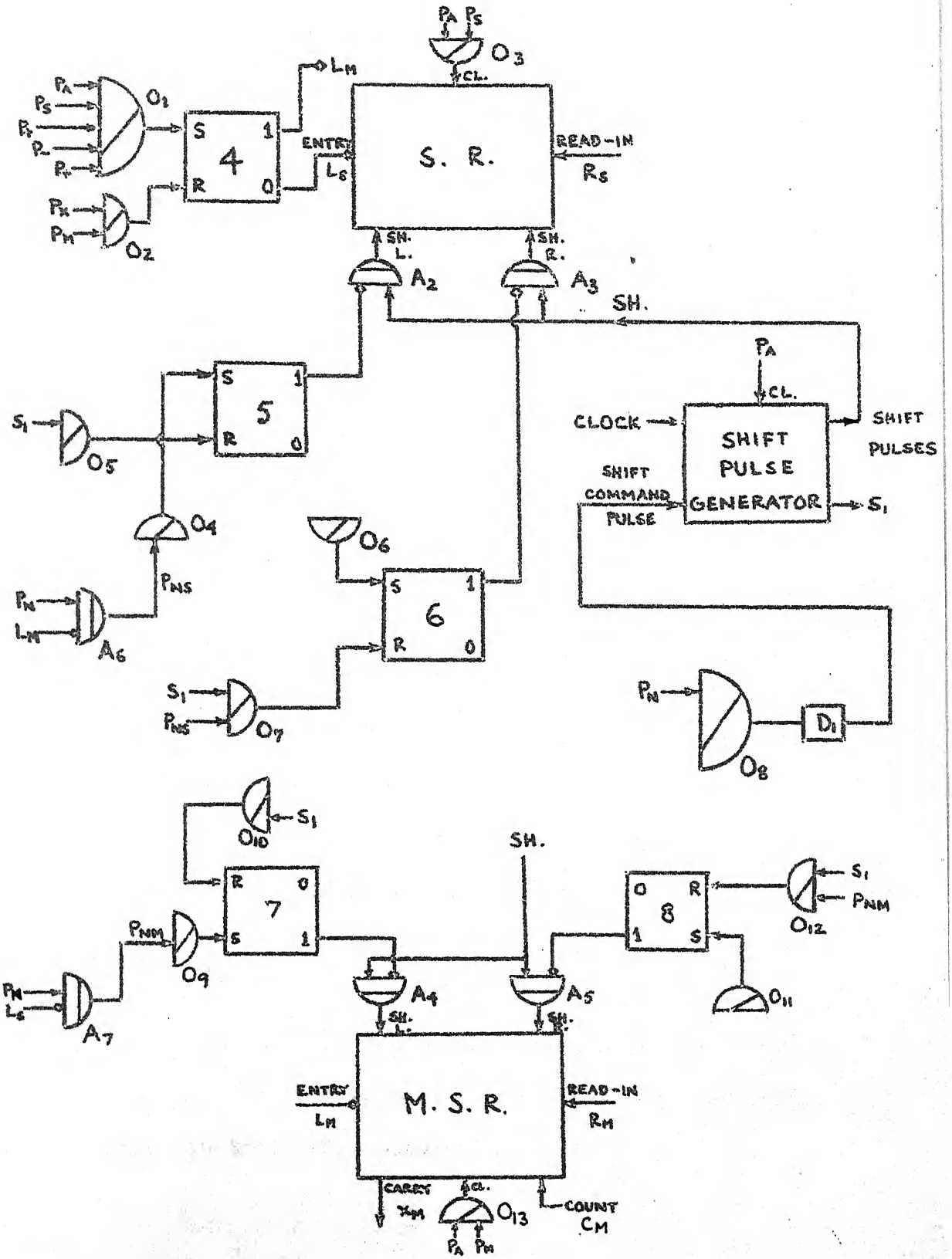

PA PS
O3
CL.
LM
PA
PS
PR
PL
PK
PM
O1
O2
S
1
4
R
0
ENTR
LS
S. R.
READ-IN
RS
SH. L.
SH. R.
A2
A3
SH.
PA
CL.
CLOCK
SHIFT PULSE GENERATOR
SHIFT PULSES
SHIFT COMMAND PULSE
S1
5
O5
O4
O6
PNS
PN
LM
A6
6
S1
PNS
O7
PN
O8
D1
O10
S1
SH.
7
R
0
S
1
PNM
O9
PK
LS
A7
A4
A5
8
O
R
1
S
S1
PNM
O12
O11
SH.
SH.
ENTRY
LM
M. S. R.
READ-IN
RM
CARRY
XM
CL.
O13
COUNT
CM
PA
PM

FIG. 4·3

P_S Pulse corresponding to "CLEAR S.R." key.

P_M " " " "CLEAR M.S.R." key.

P_+ " " " "+" "

P_- " " " "-" "

P_x " " " "x" "

$P_{\div}$ " " " "$\div$" "

P_N " " " NUMERALS keys.

SH A set of four shift pulses.

L_S Level corresponding to number entry into S.R.- enabling level is "zero" (F_4 is set).

L_M Level corresponding to number entry into M.S.R.- enabling level is 'zero' (F_4 is reset).

R_S Read-in pulse for S.R.

R_M " " " M.S.R.

X_M Carry pulse from M.S.R.

C_M Count pulses entering M.S.R.

P_{NS} P_N . L_M , i.e., digit pulses corresponding to the numbers which are entered into S.R.

P_{NM} P_N . L_S , i.e., digit pulses corresponding to the numbers which are entered into M.S.R.

4.5.3 <u>ADDITION/SUBTRACTION</u>:-

A logic diagram for the mechanisation of the process of ADDITION/SUBTRACTION has been shown in Fig. 4.4 and there are a few points to be noted, namely

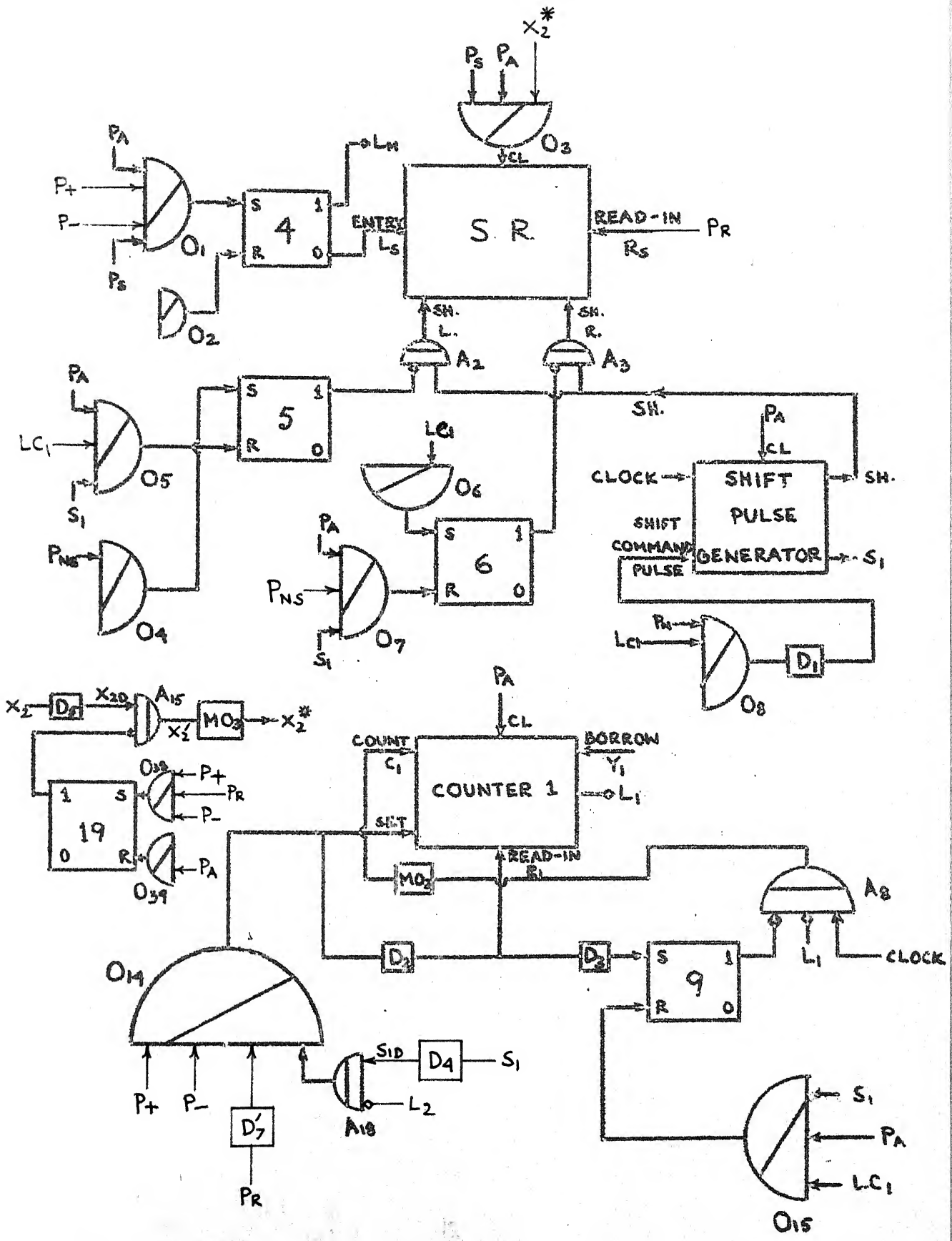


FIG. 4·4 (a) LOGIC DIAGRAM FOR ADDITION/SUBTRACTION

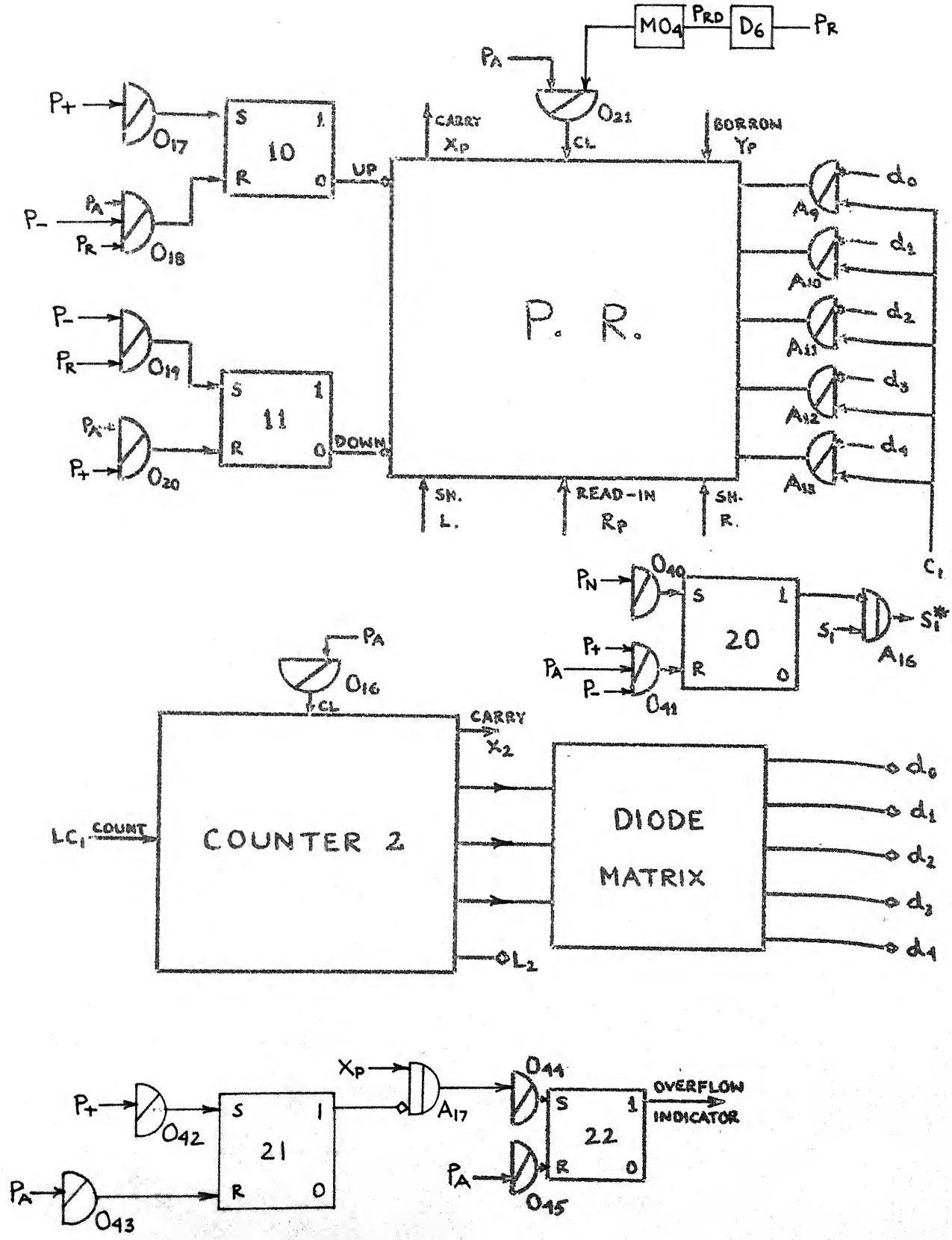


FIG. 4·4 (b) LOGIC DIAGRAM FOR ADDITION/SUBTRACTION

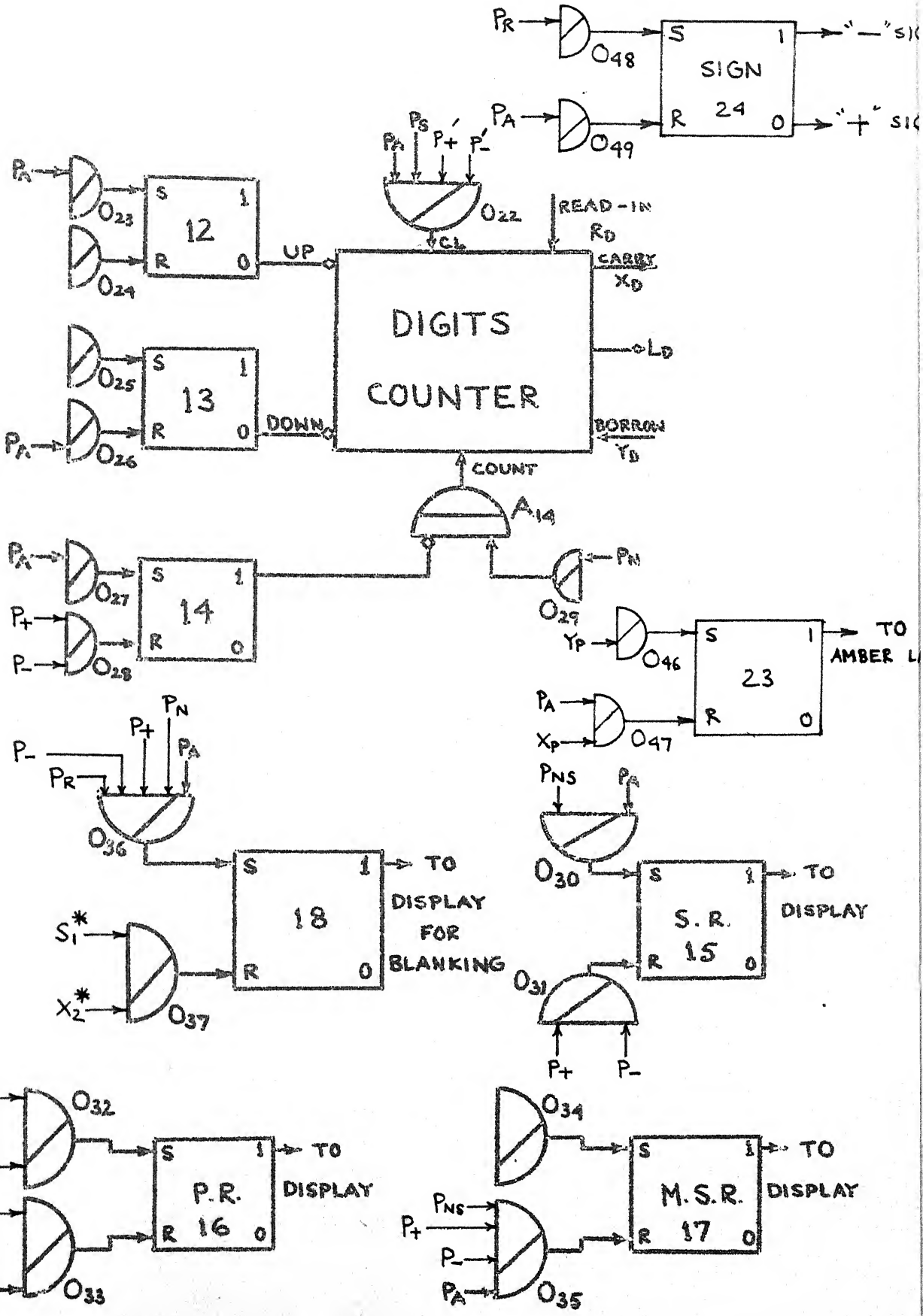


FIG. 4·4 (c) LOGIC DIAGRAM FOR ADDITION/SUBTRACTION

(i) The "+" and "−" keys on the console are "command" keys and not "sign" keys so that they should be used to add to, or subtract from, the content of P.R., the number just entered.

(ii) Only the control flip flops (and not the driving and associated circuitry) for the complement form indicating amber lamp, overflow indicating red lamp and sign indicating NIXIE tube have been shown.

(iii) Although some of the AND/OR gates with single input may appear superfluous, Yet they are actually not so because more inputs will be connected to them for the operations of Multiplication and Division.

EXPLANATION OF THE SYMBOLS USED IN FIG. 4.4:

P_R	Pulse corresponding to the "RESTORE" key.
L_1, L_2, L_D	Level outputs of the OR gates used to sense the reading of COUNTER 1, COUNTER 2 and DIGITS counter. Levels are "zero" only when the counter readings are 0 and are "one" otherwise.
C_1	Count pulses input to COUNTER 1.
R_1, R_p	Read-in pulse for COUNTER 1 and P.R. respectively.
X_2, X_p, X_D	Carry pulse obtained from COUNTER 2, P.R. and DIGITS counter respectively.
Y_1, Y_p, Y_D	Borrow pulse obtained from COUNTER 1, P.R. and DIGITS counter respectively.
LC_1	Pulse generated (from a Monostable Multivibrator) as soon as L_1 changes from "one" to "zero".

X_{2D}, S_{1D}, P_{RD} Delayed X_2, S_1 and P_R respectively.

X_2' Output of A_{15}.

X_2^* A wide pulse obtained as output from MO_3 whose input is X_2'.

S_1^* Output of A_{16}, it removes the blanking on the display after each digit has been entered and duly shifted.

4.5.4 MULTIPLICATION:-

The various symbols used in Fig. 4.5, which provides the logic design for the process of MULTIPLICATION, are defined below:

L_3, L_4 - Level outputs of the OR gates used to sense the reading of COUNTER 3, and COUNTER 4 respectively. Levels are "zero" only when the counter readings are 0 and are "one" otherwise.

R_3 - Read-in pulse for COUNTER 3.

C_3 - Count pulses input to COUNTER 3.

Y_3 - Borrow pulse obtained from COUNTER 3.

LC_3 - Pulse generated with the change of L_3 from "one" to "zero".

X_4 - Carry pulse obtained from COUNTER 4.

R_{3D}, X_{4D}, LC_{3D} - Delayed R_3, X_4 and LC_3 respectively.

X_4^* - A wide pulse generated as output from MO_6 whose input is X_{4D}.

P_X^* - A wide pulse generated from P_X.

C_{3D} - Delayed C_3.

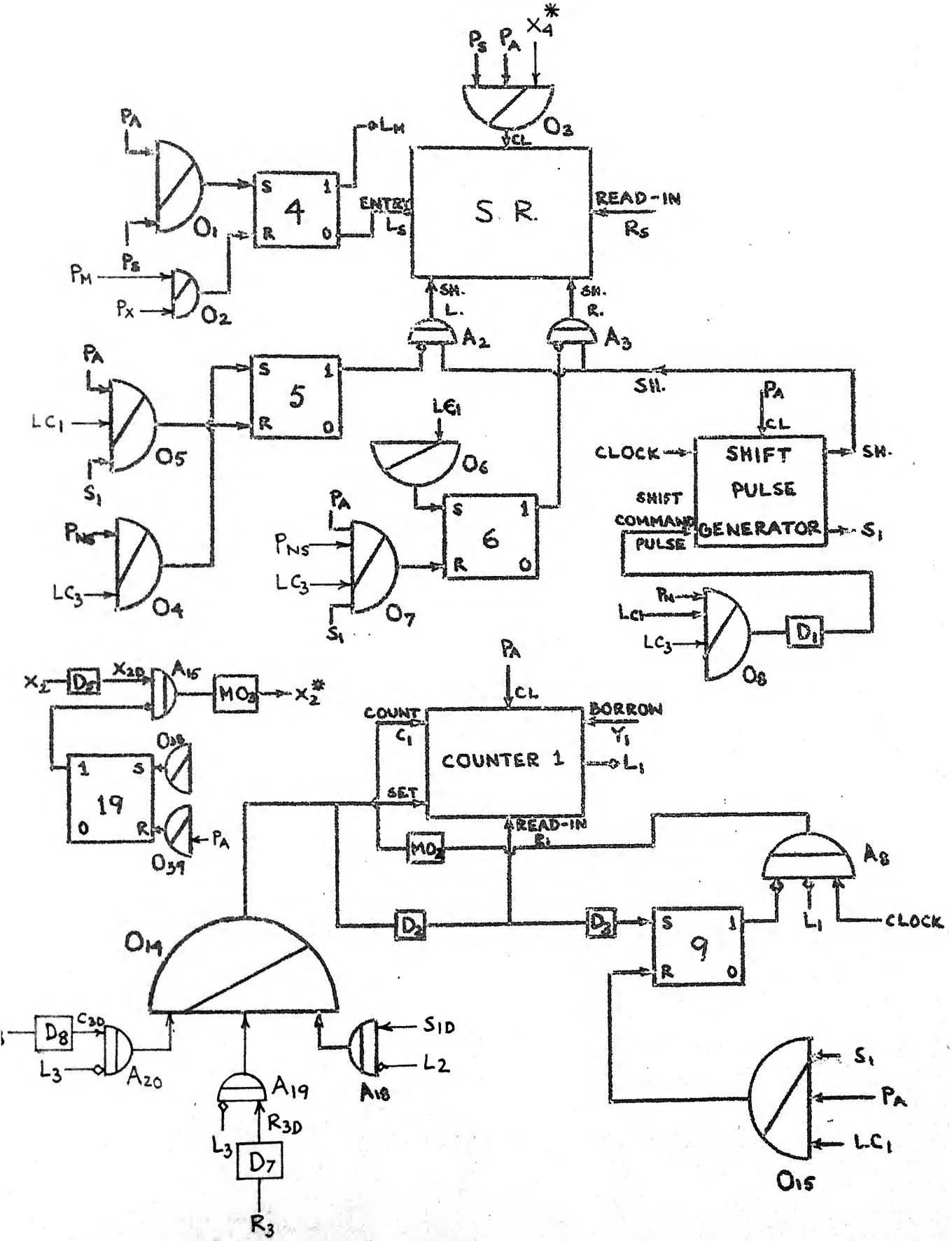


FIG. 4·5 (a) LOGIC DIAGRAM FOR MULTIPLICATION

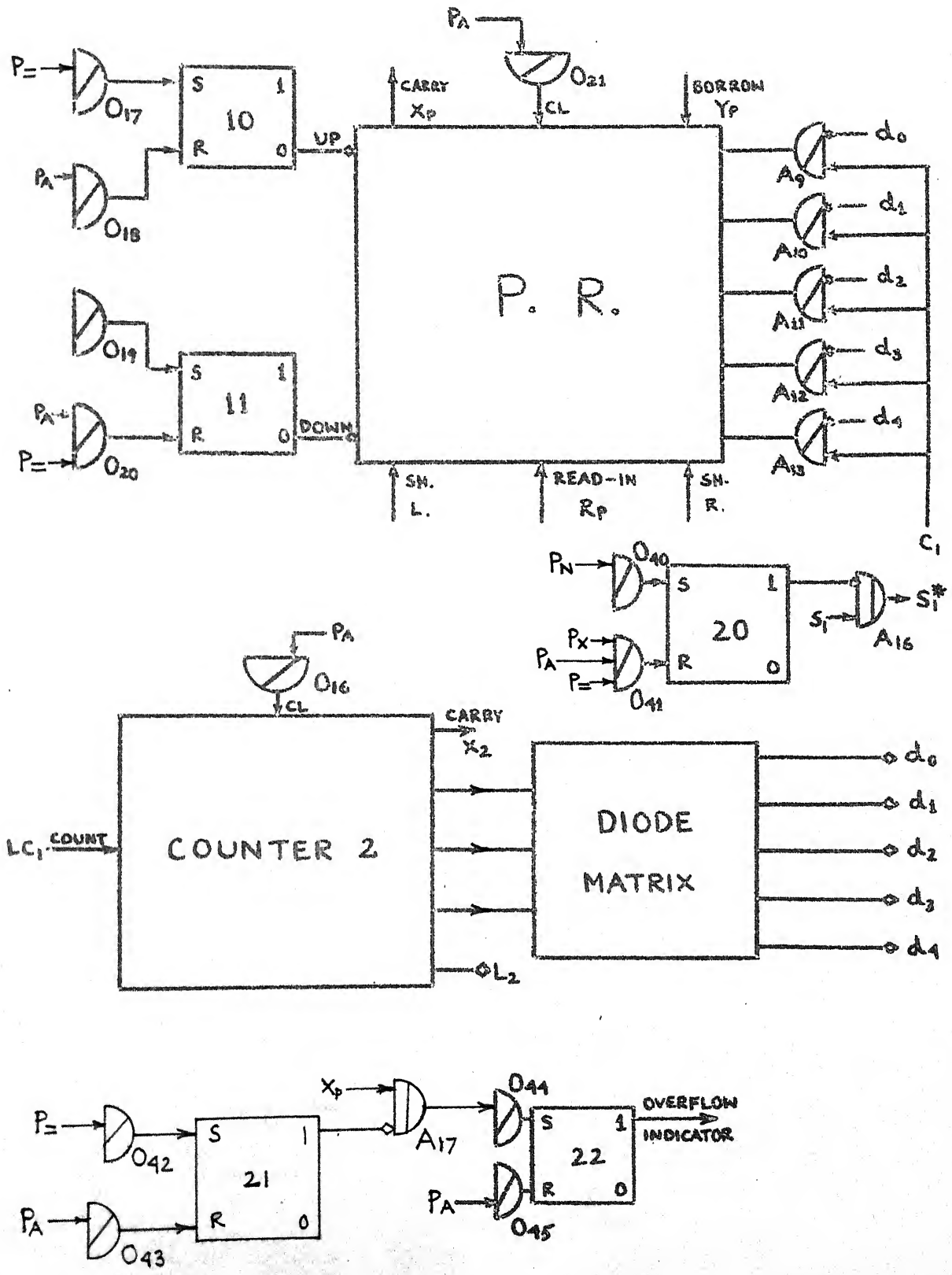


FIG. 4.5 (1) LOGIC DIAGRAM FOR MULTIPLICATION

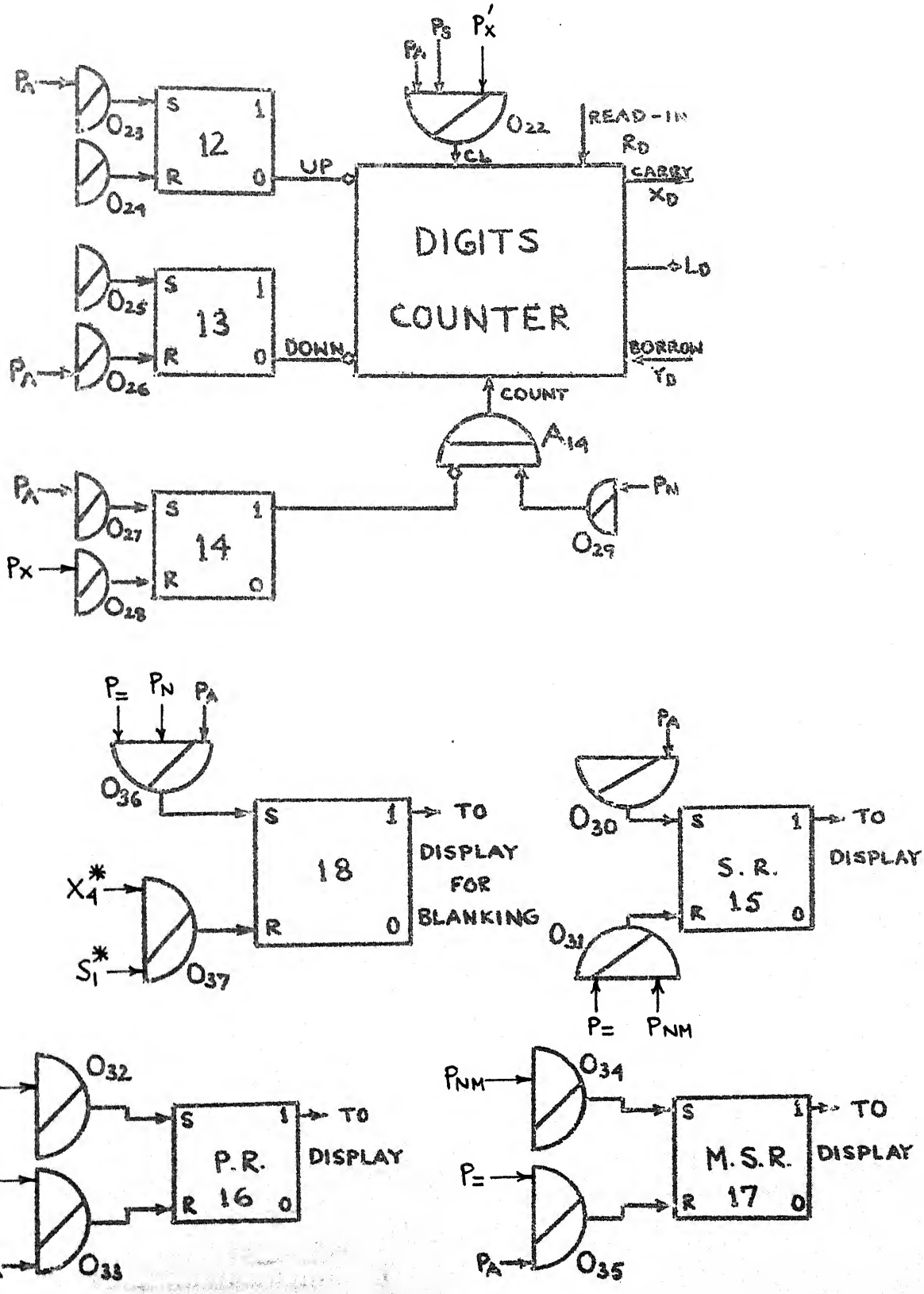


FIG. 4·5 (c) LOGIC DIAGRAM FOR MULTIPLICATION

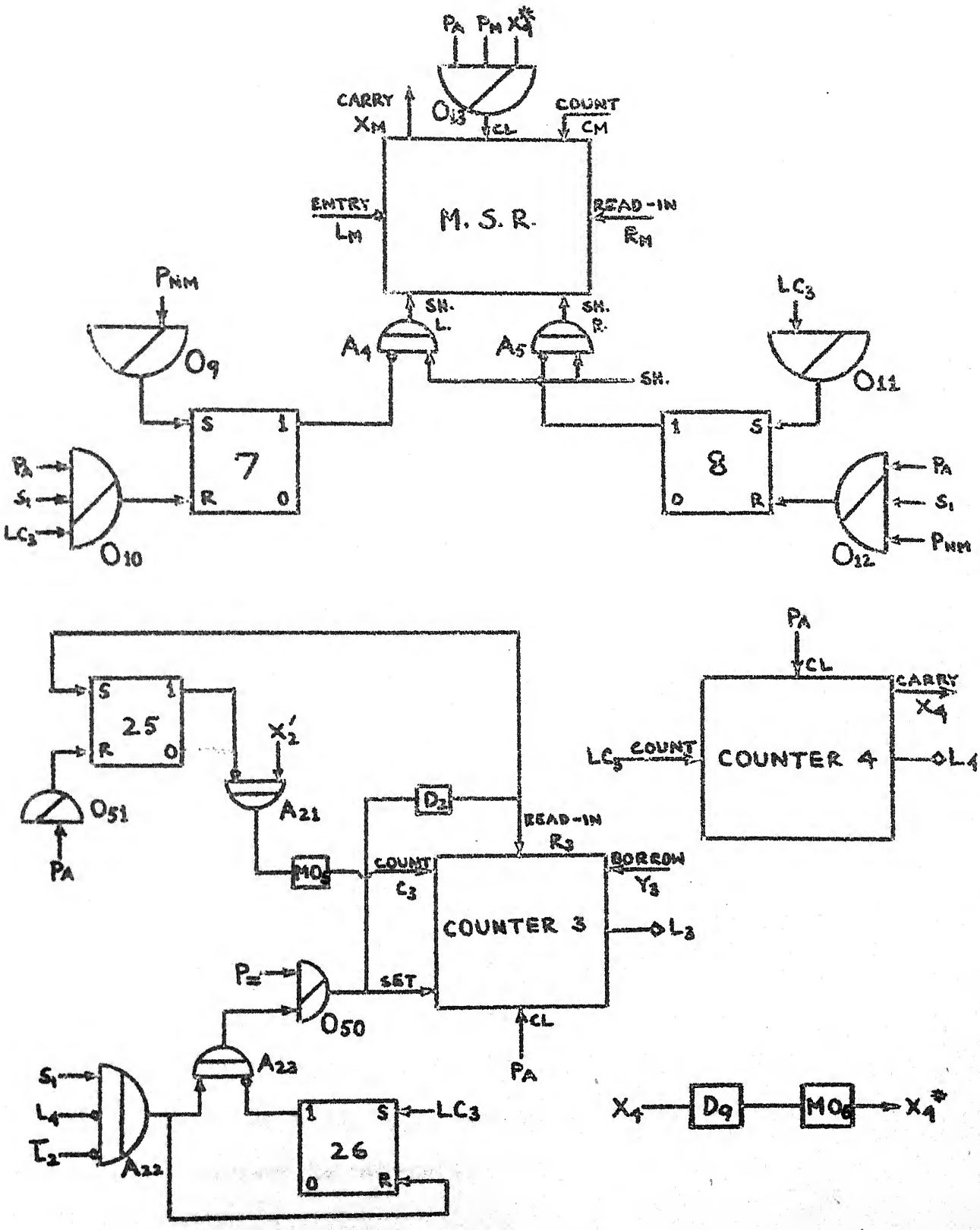


FIG 4·5(d) LOGIC DIAGRAM FOR MULTIPLICATION

Fig. 4.6 shows the logic block diagram for the process of DIVISION and below are explained the various notations used:

R_C Read-in pulse for the CORRECTION REGISTER.

R_{CH} Read-in pulse for the CHECK counter.

L_{CH} Level of the OR gate used to sense the CHECK counter reading. It is "zero" only when the counter reading is 0 and is "one" otherwise.

T_Z Level output of the AND gate used to test whether the divisor (stored in S.R.) is zero, before the start of the operation of division. (The input to this AND gate, not shown in Fig. 4.6, are the '0' line outputs of the five B C D 8-4-2-1 TO DECIMAL DECODERS, one of which shown in Fig. 3.4). T_Z is "one" only if the S.R. reads 00000 and it is "zero" otherwise.

$L_{\div}$, $L_{\neq}$ "One" outputs of the flip-flops which are set by $P_{\div}$ and $P_{\neq}$ respectively.

$P_{\neq Y} \rightarrow L_{\neq} . Y_P$, obtained as output of A_{28}.

P_{DE} Digit-equalling pulses, obtained as output from A_{27} (i.e., $S_1 . L_D . L_{\neq}$).

P_{REM} Pulse corresponding to the "REMAINDER" key.

$P_{\neq S} \rightarrow P_S . L_{\neq}$, obtained as output from A_{31}.

$L_{\neq Y}$ "One" output of F_{29} which is set by $P_{\neq Y}$.

$P'_{\neq} \rightarrow P_{\neq} . \bar{T}_Z$ Output of A_{36} and obtained only if the divisor is non-zero.

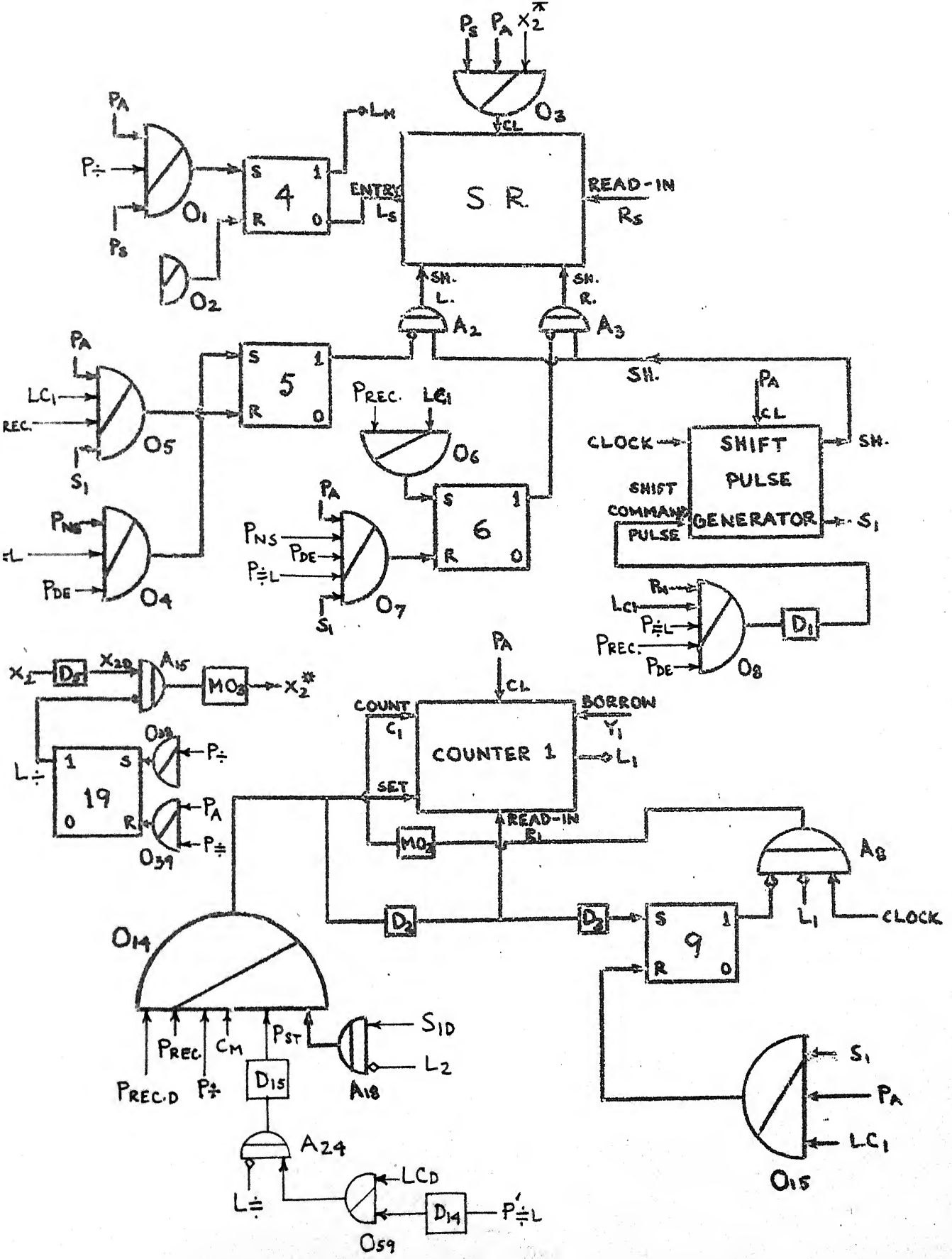


FIG. 4.6 (a) LOGIC DIAGRAM FOR DIVISION

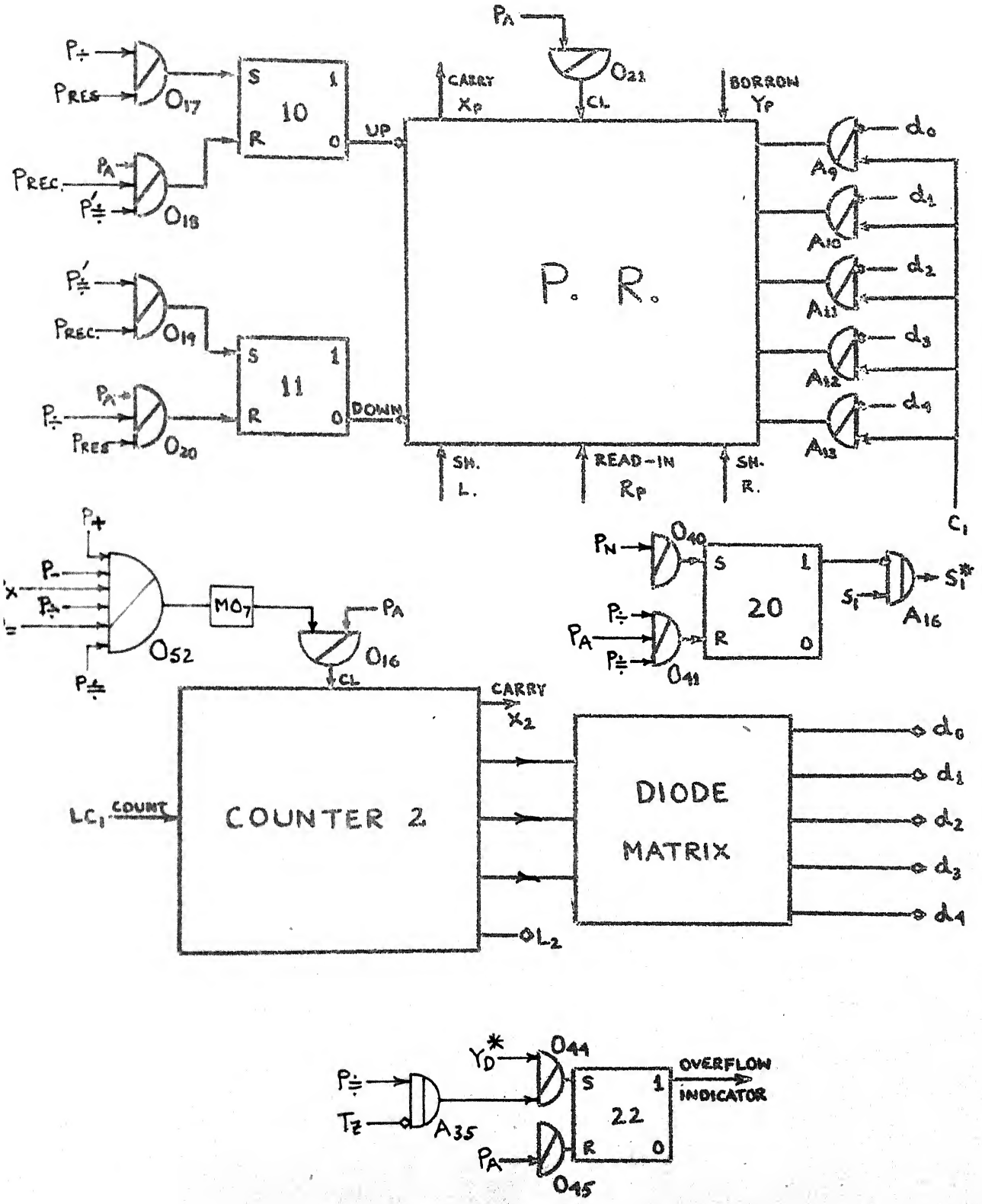


FIG. 4·6 (a) LOGIC DIAGRAM FOR DIVISION

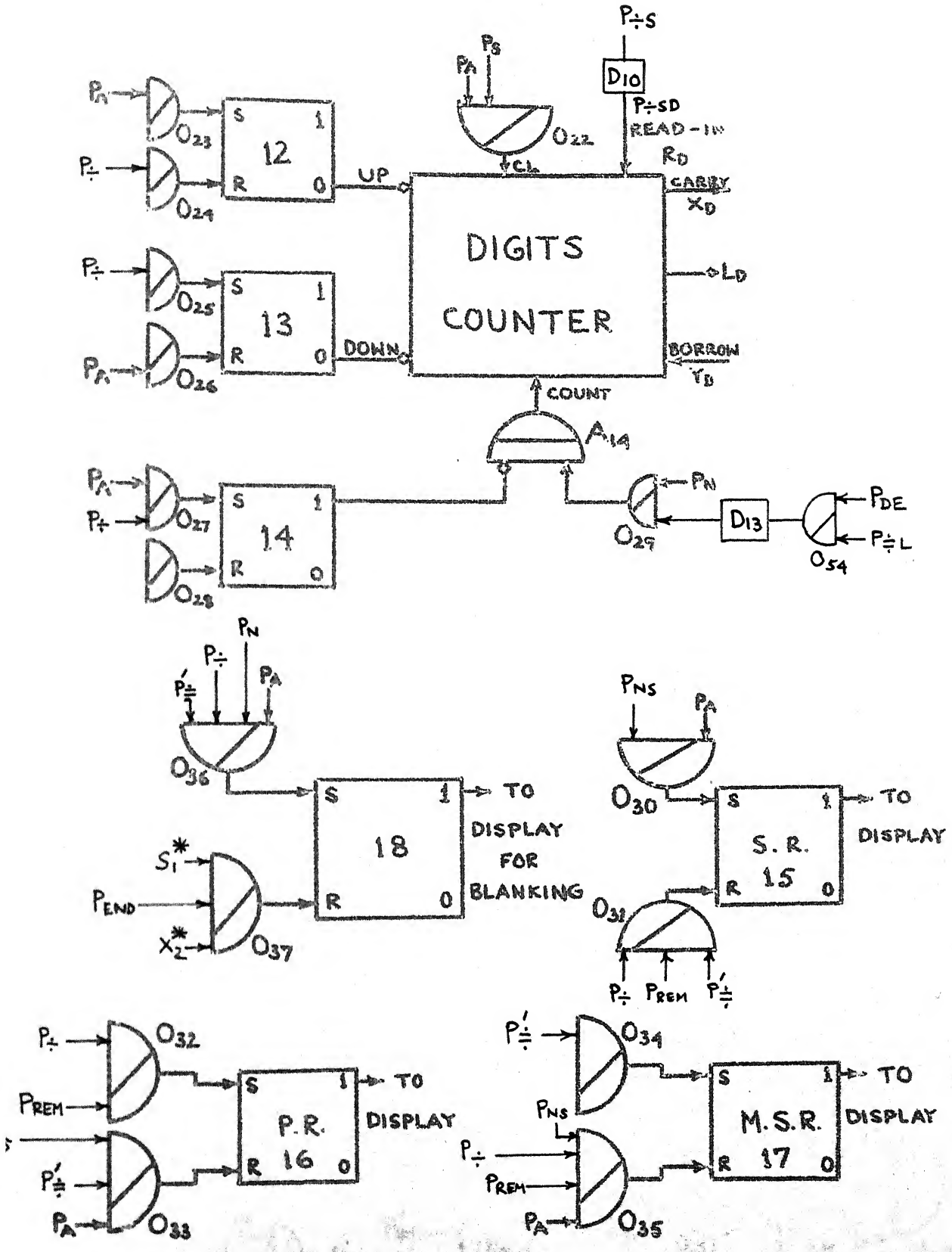


FIG. 4.6 (c) LOGIC DIAGRAM FOR DIVISION

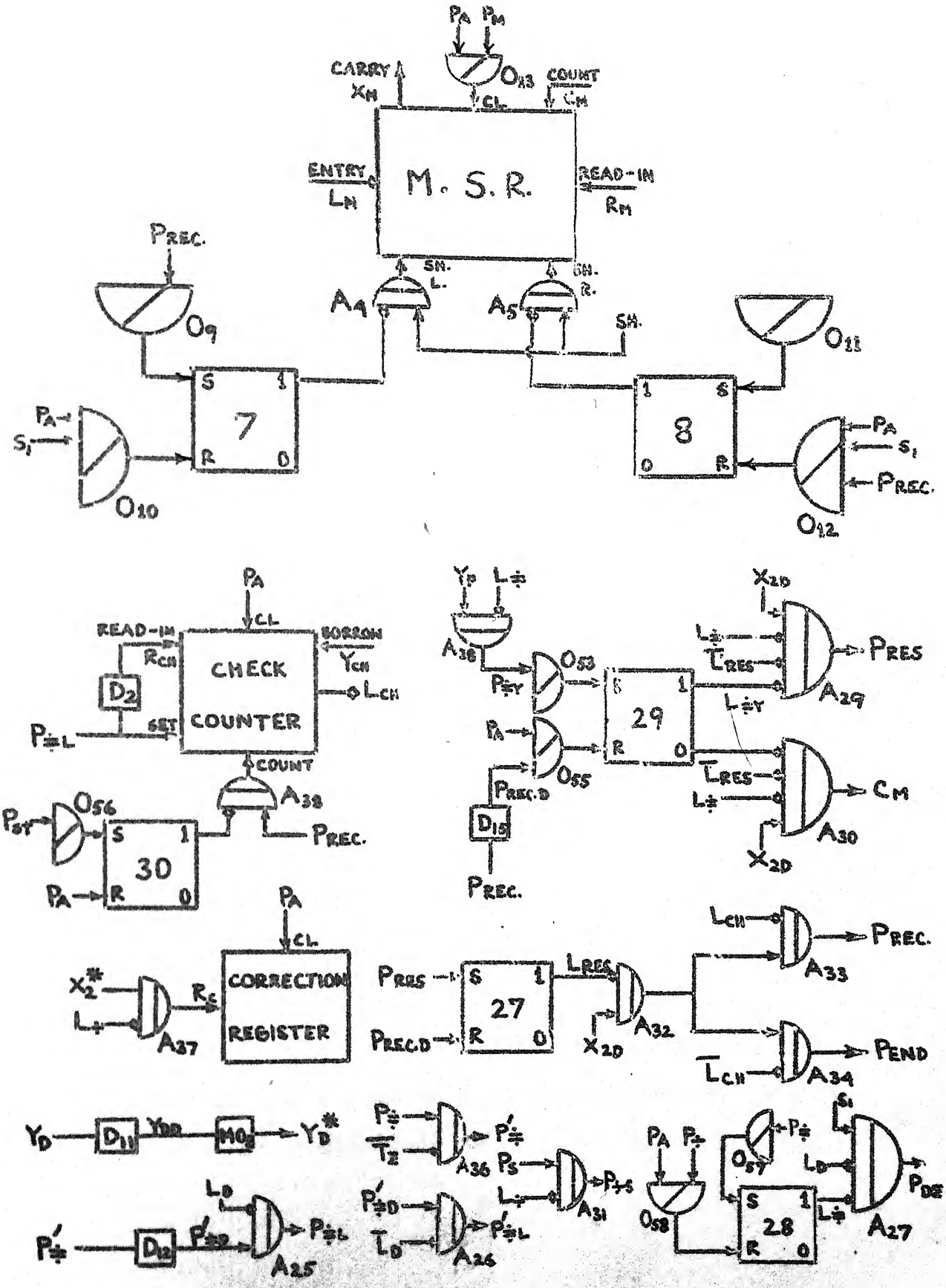


FIG. 4·6(d) LOGIC DIAGRAM FOR DIVISION

$P'_{\div D}$	$P'_{\div}$ delayed.
$P_{\div L}$	$P'_{\div D}$. L_D, obtained as output of A_{25}.
$P'_{\div L}$	$P'_{\div D}$. $\overline{L}_D$, obtained as output from A_{26}.
L_{CD}	Pulse generated with the change of L_D from "one" to "zero".
P_{ST}	Pulse which first starts the process of repeated subtraction. It is obtained as L_{CD}. $L_{\div}$ delayed ~~is~~ by D_{13}.
P_{RES}	Restoring pulse obtained as the output of A_{29}, i.e., $L_{\div}$. $L_{\div Y}$. X_{2D}. $\overline{L}_{RES}$
L_{RES}	"One" output of F_{27} which is set by P_{RES}.
P_{REC}.	$\overline{L}_{CH}$. L_{RES}. X_{2D}, obtained as output from A_{33}.
$P_{REC.D}$	Delayed P_{REC}.
P_{END}	L_{CH}. L_{RES}. X_{2D}, obtained as output of A_{34}.
Y_{DD}	Delayed Y_D.
Y_D*	A 125 μSec wide pulse generated from Y_{DD}.

4.6 DETAILED TIMING CHART FOR THE MACHINE OPERATIONS:-

The purpose of preparing this timing chart is to gain some insight into the matter of validity of the detailed logic employed for the mechanisation of the four fundamental operations. Consequently, arbitrary values (not impractical, however) have been assumed for the relevant parameters and only the functions that are important for an understanding of the machine logic have been included in the timing sequence, for obvious reasons. Moreover, though not a practical proposition, all flip-flops

have been assumed to be triggered through Diode-Capacitor-Diode (D-C-D) gates for convenience.

DATA USED:

Clock frequency - 40 K cps; Period T = 25 μ Sec.;
Pulse width - 4 μ Sec. ; Flip-flop transition time - 2 μ Sec.;
Delay introduced by AND gates, OR gates, encoders, decoders and similar blocks are much smaller than flip-flop transition time and hence has been considered as nil.
D-C-D gate delay - 3 μ Sec. ;
Total carry propagation time in S.R. or P.R. or M.S.R. is 5 x 4 x (4 +2) = 120 μ sec. (maximum). Hence CLEAR Pulses (i.e., P_A, P_S and P_M) should be about 125 μ sec. in width to override carries which would otherwise be generated from one stage to another.
All timings are in μ sec.

4.6.1 SHIFTING:- (FIG. 4.2)

Before the start it is assumed that FF_1, FF_2 and FF_3 are reset and at

t = 0 SHIFT COMMAND PULSE arrives.
t = 4 FF_3 is actually triggered.
t = 6 FF_3 flips and A_1 is enabled.
t between 6 & 30 - First shift pulse is given out (assuming no day is introduced by MO_1).
t between 31 & 55 - Second shift pulse is given out.
t " 56 & 80 - Third " " " " "

t between 81 & 105 - Fourth shift pulse is given out.

t " 93 & 117 - FF_2 changes level from "one" to "zero", and actuates the pulse generator.

Let $\boxed{D = 6}$, so that at

t between 99 & 123 - S_1 is obtained - FF_3 flops and A_1 is disabled.

t " 106 & 130 - Fifth clock pulse reaches A_1 but is blocked.

NOTE: If the SHIFT COMMAND PULSE arrives at t = 0, then the last shift pulse is given out at t between 81 & 105 so that shifting of the corresponding register is completed at t between 87 & 111 and S_1 is given out at t between 99 & 123.

4.6.2 ENTERING NUMBERS INTO S.R. OR M.S.R.:- (FIG. 4.3)

The time interval between the instants of pressing of a key and availability of the corresponding pulse at the pulse output point (Ref. Fig. 3.1) is of the order of a few milliseconds (it depends on the microswitch or the relay used); however, this delay being same for all the different keys, does not come into picture while making the timing chart.

1. PRESS "CLEAR ALL":

t = 0 P_A is available.

t = 127 (125 +2) S.R., M.S.R., SHIFT PULSE GENERATOR, etc.

are cleared - F_4 is set so that L_S becomes "zero" (i.e., S.R. is made ready to accept the next entry) and consequently L_M becomes "one" - A_6 is enabled and A_7 is disabled.

2. INDEX NUMERALS:

t = 0 P_N is available and is input to O_8 - P_{NS} is input to O_4 to set FF_5.

t = 6 FF_5 is set so that A_2 is enabled - the digit is encoded and entered into S.R. (see Fig. 3.2).

Now the delay D_1 is chosen arbitrarily as $D_1 = 10$ so that the shift pulse is input to the D-C-D gates after at least 10 micro-seconds from the time it was enabled (i.e., when the number entry into S.R. was completed). Hence at

t = 10 SHIFT COMMAND PULSE arrives.

t between 97 & 121 Fourth bit shifting, i.e., the digit shifting is completed.

t between 109 & 133 S_1 is given out.

t between 115 & 139 A_2, A_3, A_4 & A_5 are all disabled.

The above timing sequence is repeated for each numeral.

4.6.3 ADDITION/SUBTRACTION:- (FIG. 4.4)

Ex. 2031 + 72.

Since the process of adding both 2031 and 72 from the S.R. to the content of P.R. (initially 0) is same, it will be enough to provide the timing chart for the first

operand, i.e., 2031.

1. PRESS "CLEAR ALL" - In addition to what was explained corresponding to CLEAR ALL key in Section 4.6.2, at

t = 127 The DIGITS counter is cleared, enabled and set to count up - the Display unit is connected to S.R. and is blanked - the positive cathode of the NIXIE tube displaying sign is connected.

NOTE: Since the time delay T_S in the display system (i.e., the time gap between the connection of a register and actual glowing of the correct numeral) is of the order of a few milliseconds (see Fig. 3.3 & 3.4) an equal amount of delay should be introduced in the blanking circuit also in order to make the use of the latter meaningful.

2. INDEX 2031: - In addition to what was explained corresponding to "INDEX NUMERALS" in Section 4.6.2, at

t = 0 The digit pulse is input to the DIGITS counter.

t = 6 Blanking is imposed - A_{16} is enabled.

t between 109 & 133 S_1 arrives at A_{16} and S_1^* is generated.

t between 115 & 139 Blanking is withdrawn.

Thus the content of S.R. is displayed at t between $(115 + T_S)$ & $(139 + T_S)$.

3. PRESS "+" -

t = 0 P_+ is available and is applied to O_{14} to set COUNTER 1 to 9 (i.e., 1001).

t = 6 FF_{10} is set and P.R. is ready to count up - the Display is connected to P.R. and is blanked - the DIGITS counter is reset and disabled - A_{15} & A_{17} are enabled while A_{16} is disabled - L_1 becomes "one".

t = 24 COUNTER 1 is set to 9.

Let D_2 be chosen as $\boxed{D_2 = 25}$, so that at

t = 25 R_1 is input to COUNTER 1.

Also let $\boxed{D_3 = 5}$, so that at

t = 30 A pulse is input to the D-C-D gate of F_9 to set it.

t = 31 COUNTER 1 completes the reading in of the least significant digit in S.R. (i.e., 1) - L_1 remains "one".

t = 36 A_8 is enabled.

t between 37 & 61 The first count pulse is input to COUNTER 1 and the least significant counter of P.R. through A_9.

t between 43 & 67 COUNTER 1 reads 0 (i.e., 0000) - L_1 becomes "zero" disabling A_8 - LC_1 is generated - P.R. reads 00001.

t between 49 & 73 A_3 is enabled - COUNTER 2 reads 1 (i.e., 0001) so that L_2 becomes "one" and A_{10} is enabled.

t between 53 & 77 SHIFT COMMAND PULSE arrives.

t between 140 & 188 The right shifting of S.R. is completed and it reads 10203.

t between 152 & 200 S_1 is given out.

Let $D_4 = 5$, so that at

t between 157 & 205 S_{1D} is applied to O_{14}.

t between 158 & 206 A_2 and A_3 are reset - F_9 is reset so that FF_8 remains disabled.

t between 163 & 211 L_1 becomes "one".

t between 188 & 236 COUNTER 1 completes the reading in of the least significant digit in S.R. (i.e., 3) - L_1 remains "one".

t between 193 & 241 A_8 is enabled.

t between 194 & 266 The first count pulse (C_1) is input to COUNTER 1 as well as the 10's counter of P.R.

t between 244 & 316 The third C_1 pulse is input to COUNTER 1 and the 10's counter of P.R.

t between 250 & 322 COUNTER 1 reads 0 and L_1 becomes "zero" - LC_1 is generated and A_8 is disabled - P.R. reads 00031.

t between 256 & 328 A_3 is enabled - COUNTER 2 reads 2 (0010) so that L_2 remains "one" but A_{11} becomes enabled.

t between 260 & 332 SHIFT COMMAND PULSE arrives.

t between 347 & 443 The right shifting of S.R. is completed and it reads 31020.

t between 359 & 455 S_1 is given out.

t between 364 & 460 S_{1D} is applied to O_{14}.

t between 365 & 461 A_2 and A_3 are reset - A_8 is disabled.

t between 370 & 466 L_1 becomes "one".

t between 395 & 491 COUNTER 1 completes the reading in of the least significant digit in S.R. (i.e., 0) - L_1 becomes "zero" and so A_8 is disabled - LC_1 is generated.

t between 400 & 496 F_9 is set but A_8 remains disabled so that no pulse is entered into either COUNTER 1 or P.R. and P.R. reads 00031.

t between 401 & 497 A_3 is enabled - COUNTER 2 reads 3 (0011) so that L_2 remains "one" and A_{12} is enabled.

t between 405 & 501 SHIFT COMMAND PULSE arrives.

t between 492 & 612 The right shifting of S.R. is completed and it reads 03102.

t between 504 & 624 S_1 is given out.

t between 509 & 629 S_{1D} is applied to O_{14}.

t between 510 & 630 A_2 and A_3 are reset - A_8 remains disabled.

t between 515 & 635 L_1 becomes "one" but A_8 remains disabled.

t between 540 & 660 COUNTER 1 completes the reading in of the least significant digit in S.R. (i.e., 2) - L_1 remains "one".

t between 545 & 665 A_8 is enabled.

t between 546 & 690 The first count pulse (C_1) is input to COUNTER 1 as well as the 1000's place in P.R.

t between 571 & 715 The second count pulse (C_1) is input to COUNTER 1 as well as the 1000's place in P.R.

t between 577 & 721 - COUNTER 1 reads 0 and L_1 becomes "zero" - A_8 is disabled and LC_1 is generated - P.R. reads 02031.

t between 583 & 727 - A_3 is enabled - COUNTER 2 reads 4 (0100) so that L_2 remains "one" and A_{13} is enabled.

t between 587 & 731 - SHIFT COMMAND PULSE arrives.

t between 674 & 842 - The right shifting of S.R. is completed and it reads 20310.

t between 686 & 854 - S_1 is given out.

t between 691 & 859 - S_{1D} is applied to O_{14}.

t between 692 & 860 - A_2 and A_3 are reset - A_8 remains disabled.

t between 697 & 865 - L_1 becomes "one" but A_8 remains disabled.

t between 722 & 890 - COUNTER 1 completes the reading in of the least significant digit in S.R. (i.e., 0) - L_1 becomes "zero" and so A_8 remains disabled - LC_1 is generated.

t between 727 & 895 - F_9 is set but A_8 remains disabled so that no pulse is entered into either COUNTER 1 or P.R. and P.R. reads 02031.

t between 728 & 896 - A_3 is enabled - COUNTER 2 reads 0 (i.e., 0000) so that L_2 becomes zero, A_9 is enabled and L_2 is generated.

t between 732 & 900 - SHIFT COMMAND PULSE arrives.

t between 819 & 1011 - The right shifting of S.R. is completed and it reads 02031.

t between 831 & 1023 - S_1 is given out.

t between 836 & 1028 - S_{1D} is blocked by A_{18}.

t between 837 & 1029 - A_2 and A_5 are reset - A_8 remains disabled.

Only after this the S.R. should be cleared and the blanking should be withdrawn. So, X_2 which was generated at t between 728 & 896, has to be delayed by say, $\boxed{D_5 = 140}$, so that at

t between 868 & 1036 - X_{2D} and hence X_2' as well as X_2^* (125 wide) are generated.

t between 995 & 1163 - S.R. is cleared and the blanking is withdrawn.

Thus the P.R., storing 02031, is displayed at t between $(995 + T_S)$ & $(1163 + T_S)$.

NOTE: From a study of the timing chart just presented, a particular repetitive nature is observed and it comes out that

(i) there is a constant time gap of t between 114 & 138 between the generation of LC_1 and the next S_{1D}, in each digit-cycle.

(ii) The time interval between the entry of S_{1D} and the generation of corresponding LC_1 is dependent on the digit being added and this time interval is listed below for the 10 digits:

For 0	LC_1	is	generated	at	t = 31	after	the	entry	of	S_{1D}	in O_{14}
For 1	"	"	"	"	t between	43 & 67	"	"	"	"	"
For 2	"	"	"	"	t "	68 & 92	"	"	"	"	"
For 3	"	"	"	"	t "	93 & 117	"	"	"	"	"
For 4	"	"	"	"	t "	118 & 142	"	"	"	"	"

For 5 LC_1 is generated at t between 143 & 167 after the entry of S_{1D} i

For 6 " " " " t " 168 & 192 " " " "

For 7 " " " " t " 193 & 217 " " " "

For 8 " " " " t " 218 & 242 " " " "

For 9 " " " " t " 243 & 267 " " " "

(iii) X_2' is generated at t = 146 after the last LC_1 is obtained.

From the observations (i), (ii) and (iii), the "cycle time" for the addition of any number from S.R. to the content of P.R. can be computed. The maximum cycle time (for the number 99999) will be t between 1817 & 2033 microseconds.

PRESS "RESTORE":-

At t = 0 P_R is available.

t = 6 The P.R. is set to count down - the display is blanked - the negative cathode of the sign displaying NIXIE tube is connected - reading in of the content of P.R. into S.R. is completed.

Let D_6 be chosen as $\boxed{D_6 = 10}$, so that at

t = 10 P_{RD} is applied to clear P.R.

t = 137 P.R. is cleared.

Since after the initiation of an ADDITION/SUBTRACTION CYCLE, the first count pulse is input to COUNTER 1 or P.R. only after a minimum time of 37, a delay $\boxed{D_7' = 110}$ is introduced before P_R is input to O_{14} to start an ADDITION/SUBTRACTION CYCLE. Hence at t = 110 an ADDITION/SUBTRACTION CYCLE (its timing chart has already been

prepared completely) is initiated and at the end X_2^* is generated to clear S.R. and remove blanking.

4.6.4 MULTIPLICATION:-

Ex. 25 x 221

1. PRESS "CLEAR ALL" - Already explained.
2. INDEX 25 - " "
3. PRESS "X" -

t = 0 Px and Px^* (25 μsec wide) are available.

t = 6 FF_4 is reset so that L_M becomes "zero" and L_S becomes "one" - A_7 is enabled and A_6 is disabled - the DIGITS counter is disabled.

t = 27 The DIGITS counter is cleared.

4. INDEX 221 - In addition to what have been explained, at

t = 6 The display is connected to M.S.R.

5. PRESS "=" - (S.R. stores 00025 and M.S.R. stores 00221)

t= 0 $P_=$ is avialable and is input to G50 (i.e., to the D-C-D gate of the SET input to COUNTER 3).

t = 6 The P.R. is set to count up - the Display unit is connected to P.R. and is blanked - A_{17} is enabled - L_3 becomes "one".

t = 24 COUNTER 3 is set to 9 (i.e., 1001).

t = 25 R_3 is input to COUNTER 3 and to FF_{25}.

t = 31 COUNTER 3 completes the reading in of the least significant digit in M.S.R., i.e., 1 (0001) - L_3 remains "one" - A_{21} is enabled.

Let D_7 be chosen as $\boxed{D_7 = 10}$, so that at

t = 35 R_{3D} passes through A_{19} and starts an ADDITION/SUBTRACTION CYCLE.

Now, for 00025 the ADDITION/SUBTRACTION CYCLE time is computed as t between 906 & 1050. So, at

t between 941 & 1085 - X_2' is generated and applied to A_{21} as well as D_8.

t between 947 & 1091 - COUNTER 3 reads zero and L_3 becomes "zero" - A_{19} and A_{20} are disabled - LC_3 is generated.

NOTE: D_8, which will be chosen afterwards, is more than 6, so that the ADDITION/SUBTRACTION is not repeated without sensing the COUNTER 3 reading.

t between 953 & 1097 - A_2 and A_5 are enabled - COUNTER 4 reads 1 (0001) so that L_4 becomes "one" and A_{22} is enabled - FF_{26} is set and A_{23} is enabled.

t between 957 & 1101 - SHIFT COMMAND PULSE arrives.

t between 1044 & 1212 - Digit shifting is completed - S.R. reads 00250 and M.S.R. reads 10022.

t between 1056 & 1224 - S_1 is given out and is applied to A_{22} and hence to the D-O-D gate of the SET input to COUNTER 3.

t between 1062 & 1230 - L_3 becomes "one" and A_{19} is enabled - A_{23} is disabled.

t between 1087 & 1255 - COUNTER 3 completes the reading-in of the least significant digit in M.S.R. (i.e., 2) - L_3 remains "one".

t between 1091 & 1259 - R_{3D} passes through A_{19} and starts an ADDITION/SUBTRACTION CYCLE.

t between 1997 & 2309 - X_2' is generated and applied to A_{21} (i.e., as C_3) and D_8.

t between 2003 & 2315 - L_3 remains "one" as COUNTER 3 does not read 0 - A_{20} and A_{19} remain enabled.

Let D_8 be chosen as $\boxed{D_8 = 10}$, so that at

t between 2007 & 2319 - C_{3D} is applied to O_{14} and an ADDITION/SUBTRACTION CYCLE is repeated.

t between 2913 & 3369 - X_2' is generated and applied to A_{21} as C_3 as well as to D_8.

t between 2919 & 3375 - COUNTER 3 reads 0 and L_3 becomes "zero" - A_{19} and A_{20} are disabled - LC_3 is generated.

t between 2925 & 3381 - A_2 and A_5 are enabled - COUNTER 4 reads 2 (i.e., 0010) - L_4 remains "one" and A_{22} is enabled - FF_{26} is set and A_{23} is enabled.

t between 2929 & 3385 - SHIFT COMMAND PULSE arrives.

t between 3016 & 3496 - Digit shifting is completed - S.R. reads 02500 while M.S.R. reads 21002.

t between 3028 & 3508 - S_1 is given out and is applied to A_{22} and hence to the SET input of COUNTER 3.

t between 3063 & 3543 - R_{3D} passes through A_{19} and starts an ADDITION/SUBTRACTION CYCLE.

t between 3969 & 4593 - X_2' is generated and is entered as C_3 and is also input to D_8.

t between 3979 & 4603 - C_{3D} is applied to O_{14} and an ADDITION/SUBTRACTION CYCLE is repeated.

t between 4885 & 5653 - X_2' is generated and applied to A_{21} as C_3 as well as to D_8.

t between 4891 & 5659 - COUNTER 3 reads 0 and L_3 becomes "zero" - A_{19} and A_{20} are disabled - LC_3 is generated.

t between 4897 & 5665 - A_2 and A_5 are enabled - COUNTER 4 reads 3 (i.e., 0011) - L_4 remains "one" and A_{22} is enabled - A_{23} is enabled.

t between 4901 & 5669 - SHIFT COMMAND PULSE arrives.

t between 4988 & 5780 - Digit shifting is completed - S.R. reads 25000 and M.S.R. reads 22100.

t between 5000 & 5792 - S_1 is given out and applied to A_{22} and hence to the SET input of COUNTER 3.

t between 5006 & 5798 - L_3 becomes "one" and enables A_{19} - A_{23} is disabled.

t between 5025 & 5817 - R_3 is input to COUNTER 3.

t between 5031 & 5823 - COUNTER 3 completes the reading in of the least significant digit in M.S.R., i.e., 0 (0000) - L_3 becomes "zero" and disables A_{19} and A_{20} - LC_3 is generated.

t between 5035 & 5827 - R_{3D} cannot pass through A_{19} and so no ADDITION/SUBTRACTION CYCLE is started.

t between 5037 & 5829 - A_2 and A_5 are enabled - COUNTER 4 reads 4 (i.e., 0100) - L_4 remains "one" - A_{23} is enabled.

t between 5041 & 5833 - SHIFT COMMAND PULSE arrives.

t between 5128 & 5944 - Digit shifting is completed - S.R. reads 50002 while M.S.R. reads 02210.

t between 5140 & 5956 - S_1 is given out and is input to the SET input of COUNTER 3.

t between 5146 & 5962 - L_3 becomes "one" and A_{19} is enabled - A_{23} is disabled.

t between 5171 & 5987 - COUNTER 3 completes the reading in of the least significant digit in M.S.R., i.e., 0 (0000) - L_3 becomes "zero" and disables A_{19} and A_{20} - LC_3 is generated.

t between 5175 & 5991 - R_{3D} cannot pass through A_{19} and consequently no ADDITION/SUBTRACTION CYCLE is started.

t between 5177 & 5993 - A_2 and A_5 are enabled - COUNTER 4 reads 0 and X_4 is given out - L_4 becomes "zero" thus disabling A_{22} - A_{23} is enabled.

t between 5181 & 5997 - SHIFT COMMAND PULSE arrives.

t between 5268 & 6108 - Digit shifting is completed - S.R. reads 00025 and M.S.R. reads 00221.

t between 5280 & 6120 - S_1 is given out - it is applied to A_{22} but is blocked so that the operation of MULTIPLICATION is completed.

Only after this S.R. and M.S.R. can be cleared and the blanking can be withdrawn from the display. So, let D_9 be chosen as $\boxed{D_9 = 140}$. Thus at

t between 5317 & 6153 - X_{4D} is obtained and is input to MO_6 to generate X_4^* of width 125.

t between 5444 & 6260 - S.R. as well as M.S.R. are cleared and the blanking is withdrawn.

So, the P.R., storing the product 05525, is displayed at t between (5444 + T_S) and (6260 + T_S).

NOTE:- As in the case of ADDITION/SUBTRACTION, in the case of MULTIPLICATION also, a particular repetitive nature, as borne by the following observations, is present.

(i) There is a constant time gap of t between 109 & 133 between the generation of LC_3 and the next S_1 (which starts a new series of ADDITION/SUBTRACTION CYCLE).

(ii) The time interval between the start of a series of ADDITION/SUBTRACTION CYCLE (i.e., S_1) and the generation of corresponding LC_3 is dependent on the digit read into COUNTER 3 and is given by

31 + n x (ADDITION/SUBTRACTION CYCLE time + 10),

where n = 0 , ... 9.

(iii) X_{4D} is generated at t = 146 after the last LC_3 is obtained.

From the observations (i), (ii) and (iii), the "cycle time" for any MULTIPLICATION operation can be computed. Obviously, the maximum multiplication cycle time will be of the order of 10 milliseconds.

4.6.5 DIVISION:- (FIG. 4.6)

Ex. $8295 \div 23 = 360\ \frac{15}{23}$

1. PRESS "CLEAR ALL" - Already explained.

2. INDEX 8295 - Already explained.

3. PRESS "÷" -

t = 0 $P_{\div}$ is available and is applied to O_{14} to initiate an ADDITION/SUBTRACTION CYCLE.

t = 6 P.R. is ready to count up - the DIGITS counter is set to count down - the display is connected to P.R. and is blanked - FF_{19} is set to make $L_{\div}$ "one" so that A_{15} and A_{31} are enabled.

Now, computation brings out that the ADDITION/SUBTRACTION CYCLE time for 08295 will be t between 1301 & 1493 (Ref. Section 4.6.3), so that at

t between 1301 & 1493 - X_{2D} and hence X_2' is available - X_2^* is generated.

t between 1307 & 1499 - The CORRECTION REGISTER reads-in the content of the DIGITS counter.

t between 1428 & 1620 - S.R. is cleared and the blanking on the display is withdrawn.

4-A. INDEX 28 - Already explained.

(NOTE: This is a wrong entry and has been included to demonstrate the machine behaviour in such a case).

4-B. PRESS "CLEAR S.R." -

t = 0 P_S is available and $P_{\div S}$ is generated.

t = 127 S.R. as well as the DIGITS counter are cleared.

Let D_{10} be chosen as $\boxed{D_{10} = 5}$, so that at

t = 132 R_D is applied to the DIGITS counter.

t = 138 The DIGITS counter completes the reading-in of the content of the CORRECTION REGISTER.

t = 10 $P_{\neq L}$ is generated if the DIGITS counter reading is non-zero - $P'_{\neq L}$ is generated if the digit counter reading is zero - $P_{\neq L}$ is applied to the SET input of the CHECK counter, 0_4, 0_8 and 0_{54} - $P'_{\neq L}$ is input to D_{14}.

t = 16 A_2 is enabled - L_{CH} becomes "one".

t = 20 SHIFT COMMAND PULSE arrives.

t = 28 CHECK counter is set to 4 (i.e., 100).

t = 35 R_{CH} is applied.

t = 41 CHECK counter reads-in 2 from the DIGITS counter. Let D_{13} be chosen as $\boxed{D_{13} = 90}$; so at

t = 100 A COUNT pulse is input to the DIGITS counter, reading 2.

t = 106 The DIGITS counter does not read 0 and L_D remains "one", keeping A_{27} enabled.

t between 107 & 131 - The first left shifting of S.R. is completed and it reads 00230.

t between 119 & 143 - S_1 is given out and generates a P_{DE} pulse which is applied to 0_4, 0_8 and 0_{54}.

t between 129 & 153 - SHIFT COMMAND PULSE arrives.

t between 209 & 233 - A COUNT pulse is input to the DIGITS counter, reading 1.

t between 215 & 239 - The DIGITS counter reads 0 and L_D becomes "zero" - L_{CD} is generated and is input to 0_{59} and hence A_{24}.

t between 216 & 264 - The second left shifting of S.R. is completed and it reads 02300.

t between 228 & 276 - S_1 is given out but no P_{DE} is generated.

At this stage, D_{14} and D_{15} have to be chosen. D_{14} is chosen as $\boxed{D_{14} = 230}$ so that delayed $P'_{\div L}$ arrives at A_{24} around the same time as L_{GD}. D_{15} is chosen as $\boxed{D_{15} = 40}$. Thus at

t between 255 & 280 - P_{ST} is available - P_{ST} is applied to O_{14} to start an ADDITION/SUBTRACTION CYCLE as well as to the SET input of FF_{30}.

t between 261 & 286 - CHECK counter is enabled to count down.

Now, the ADDITION/SUBTRACTION CYCLE time for 02300 is computed and found to be t between 850 & 998 (Ref. Section 4.6.3), so that at

t between 1105 & 1278 - X_{2D} is given out - X_{2D} is input to A_{30} (enabled) and generates a C_M pulse - the C_M pulse enters M.S.R. and is input to O_{14} to start a second ADDITION/SUBTRACTION CYCLE.

t between 1955 & 2276 - X_{2D} is given out - a C_M pulse is generated, entered into M.S.R. and used to start a third ADDITION/SUBTRACTION CYCLE.

In a similar way, at

t between 2805 & 3274 - A fourth ADDITION/SUBTRACTION CYCLE is started.

During the fourth cycle, a Y_p pulse is generated (Ref. Section 4.2.4) whose time of occurrence cannot be known precisely and which enables A_{29} (at the same time disabling A_{30}).

t between 3655 & 4272 - X_{2D} is given out at the completion of the fourth cycle - No C_M pulse, but a P_{RES} pulse, is generated - P_{RES} is applied to O_{17}, the SET input of FF_{27} and O_{14} (to start an ADDITION/SUBTRACTION CYCLE).

t between 3661 & 4278 - P.R. becomes ready to count up - L_{RES} becomes "one" thus <u>disabling both A_{29} and A_{30} but enabling A_{32}</u>.

t between 4505 & 5270 - The ADDITION/SUBTRACTION CYCLE is completed and X_{2D} is obtained - X_{2D} finds A_{32} as well as A_{33} enabled (CHECK counter reading being 2) and hence generates a P_{REC} pulse - P_{REC} is input to O_{19}, O_6, O_9, O_8, A_{38} and D_{16}.

t between 4511 & 5276 - A_3 and A_4 are enabled - P.R. is set to count down - CHECK counter reads 1 after counting down so that L_{CH} remains "one" and <u>A_{33} remains enabled.</u>

t between 4515 & 5280 - SHIFT COMMAND PULSE arrives.

t between 4602 & 5391 - Right shifting of S.R. and left shifting of M.S.R. are completed.

t between 4614 & 5403 - S_1 is given out but <u>becomes insignificant.</u>

Let D_{16} be chosen now as $\boxed{D_{16} = 125}$, so that at

t between 4630 & 5395 - $P_{REC.D}$ is obtained - $P_{REC.D}$ is input to O_{14} to start an ADDITION/SUBTRACTION CYCLE and also to O_{55} and the RESET terminal of FF_{27}.

t between 4636 & 5401 - A_{30} is enabled while A_{29} and A_{32} are disabled.

t between 5480 & 6393 - X_{2D} is given out and generates a C_M pulse - the C_M pulse is entered into M.S.R. and is input to O_{14} to start a second ADDITION/SUBTRACTION CYCLE.

In the same way, the ADDITION/SUBTRACTION CYCLE is repeated six more times and during the seventh cycle a borrow Y_P is obtained.

t between 6330 & 7391 - Second ADDITION/SUBTRACTION CYCLE is complet

t between 7180 & 8389 - Third " " " "

t between 8030 & 9387 - Fourth " " " "

t between 8880 & 10385- Fifth " " " "

t between 9730 & 11383- Sixth " " " "

t between 10580 & 12381- Seventh ADDITION/SUBTRACTION CYCLE is completed and X_{2D} is given out - since a Y_P was generated during this cycle, a P_{RES} pulse is produced - P_{RES} is applied to O_{17}, the SET input of FF_{27} and O_{14} (to start an ADDITION/SUBTRACTION CYCLE).

t between 10586 & 12387 - P.R. becomes ready to count up - L_{RES} becomes "one" so that both A_{29} and A_{30} are disabled but A_{32} is enabled.

t between 11430 & 13379 - X_{2D} is obtained - X_{2D} passes through A_{32} and A_{33} (the CHECK counter reading being 1) to generate a P_{REC} pulse - P_{REC} is input to O_{19}, O_6, O_9, O_8, A_{38} and D_{16}.

t between 11436 & 13385 - A_3 and A_4 are enabled - P.R. is set to count down - CHECK counter reads 0 so that L_{CH} becomes "zero" thus disabling A_{33} but enabling A_{34}.

Now, the right shifting of S.R. as well as the left shifting of M.S.R. are completed and S_1 is given out. (The time sequence of these have not been included to avoid repetitions). So, at

t between 11555 & 13504 - $P_{REC.D}$ is obtained - $P_{REC.D}$ is input to O_{14} to start an ADDITION/SUBTRACTION CYCLE and also to O_{55} and the RESET input of FF_{27}.

t between 11561 & 13510 - A_{30} is enabled while A_{29} and A_{32} are disabled.

t between 12405 & 14502 - X_{2D} is given out - since a Y_P was generated during the ADDITION/SUBTRACTION CYCLE, instead of a C_M, a P_{RES} pulse is produced - P_{RES} is applied to O_{17}, the SET input of FF_{27} and O_{14} (to start an ADDITION/SUBTRACTION CYCLE).

t between 12411 & 14508 - P.R. becomes ready to count up - L_{RES} becomes "one" so that both A_{29} and A_{30} are disabled but A_{32} is enabled.

t between 13255 & 15500 - X_{2D} is obtained - X_{2D} passes through A_{32} and A_{34} (since L_{CH} is "zero") to generate the P_{END} pulse.

Thus the DIVISION CYCLE is completed, and at

t between 13261 & 15506 - The blanking on the display is withdrawn so that M.S.R., containing the quotient,

i.e., 00360, is disabled.

6. PRESS "REMAINDER" -

t = 0 P_{REM} is available and applied to O_{32}.

t = 6 The display is connected to P.R. and P.R., containing the remainder, i.e., 15, is displayed.

NOTE: A study of the timing chart for the DIVISION CYCLE reveals that the maximum "cycle time for division" will be quite high - of the order of 100 milliseconds.

4.7 ESTIMATION OF THE COMPONENT COST FOR THE PROPOSED MACHINE:-

In this Section a very rough estimation of the total cost (in Rupees) of components to be used has been presented to satisfy the readers' interest. This estimation is in no way detailed and is based on "only partially reliable" informations regarding component prices on one hand, and on the supposed use of simple and standard circuit techniques on the other hand; consequently, little authenticity or accurateness is claimed.

The entire component cost will be computed under the following six "heads":

1. INPUT SYSTEM
2. DISPLAY UNIT
3. THE DIFFERENT REGISTERS AND COUNTERS
4. LOGIC AND ASSOCIATED CIRCUITRY
5. POWER SUPPLY AND SYSTEM CLOCK
6. MISCELLANEOUS.

According to informations available, a good silicon

switching transistor presently costs Rs.13.00 while the price of a standard diode is about Rs.1.30. Also, it is gathered that a NIXIE tube and a relay (or microswitch), conforming to desired specifications, will cost around Rs.100.00 and Rs.25.00 respectively. Cost of a resistance or a capacitance need not be considered individually for obvious reasons. So, with these informations, cost per each of the basic modules, as listed below, can be estimated:

a) Flip-flop - 2 transistors + 2 diodes + a few resistances and capacitances: Rs.35.00

b) D-C-D- gate - 5 diodes + a few resistances and capacitances: Rs.8.00

c) Encoder/Decoder - About 25 diodes on the average + a few resistances and capacitances: Rs.50.00

d) TRIXIE Driver - 1 Transistor + a few resistances and capacitances: Rs.15.00

e) Controlled Pulse Generator - Rs.100.00

f) Monostable Multivibrator - Rs.35.00

g) Delay - on the average Rs.75.00

h) 3-input AND/OR gate - Rs.5.00

Now, the total "per head" cost is estimated as illustrated below:

1. INPUT SYSTEM:

25 relays → 25 x 25 = 625; 2 pulse generators →2 x 100 = 200;

1 encoder →1 x 50 = 50; Approximate Total: Rs.1000.00

2. DISPLAY UNIT:

6 NIXIE tubes →6 x 100 = 600; 50 TRIXIE drivers →50 x 15 = 750;

5 decoders → 5 x 50 = 250; 50 relays → 50 x 25 = 1250;

Approximate Total: Rs.3000.00

3. THE DIFFERENT REGISTERS AND COUNTERS:

A. THREE REGISTERS - P.R., S.R. and M.S.R.: It will be assumed that per each flip-flop 2 D-C-D gates are needed for left shifting, 2 for right shifting, 2 for counting up, 2 for counting down and 1 for reading-in. So, on the average, 8 D-C-D- gates are needed per each flip-flop in the three registers - P.R., S.R. and M.SR. Hence the cost per each register will be

20 flip-flops with D-C-D gates → 20 x (35 + 8 x 8) = 20 x 99= 2000; Approximate Total for three registers: 3 x 2000 = Rs.6000.00

B. COUNTER 1	4 x (35 + 8 x 3)	=	Rs.240.00
C. COUNTER 3	"	=	Rs.240.00
D. COUNTER 2	3 x (35 + 8 x 2)	=	Rs.150.00
E. COUNTER 4	"	=	Rs.150.00
F. DIGITS COUNTER	4 x (35 + 8 x 5)	=	Rs.300.00
G. CORRECTION REGISTER	3 x (35 + 8 x 1)	=	Rs.130.00
H. CHECK COUNTER	2 x (35 + 8 x 3)	=	Rs.120.00
APPROXIMATE TOTAL FOR HEAD 3:			Rs.7500.00

4. LOGIC AND ASSOCIATED CIRCUITRY:

60 OR gates → 60 x 5 = 300; 50 AND gates →50 x 5 = 250;

50 flip-flops → 50 x (35 + 8 x 2) = 2500; 10 MO's → 10 x 35 = 350;
20 delays → 20 x 75 = 1500; APPROXIMATE TOTAL: Rs.5000.00

5. POWER SUPPLY AND SYSTEM CLOCK:

Power Supply → 1000 ; System Clock → 250 ;

APPROXIMATE TOTAL: Rs.1250.00

6. MISCELLANEOUS:

Cabinet, mechanical fittings, indicating lamps, etc.
all taken together - APPROXIMATE TOTAL: Rs.1000.00

Hence the component cost for the entire desk calculator will be about Rs.19,000.00. However, in practice, the cost can be reduced by

(i) developing an indigeneous display system, and

(ii) doing away with the D-C-D gates at least partially, if not completely.

CHAPTER - V

5.1 SPECIFICATIONS OF A MORE SOPHISTICATED MACHINE:-

The principles and ideas developed in the earlier chapters will be extended to the design of a more sophisticated desk calculator which, with the introduction of a few special features coupled with suitable modifications, will hopefully be a commercially feasible machine. The machine, which will have a capacity : 10 x 60 x 10 (see Section 1.5) will be able to carry out the operations of Mixed Addition and Subtraction, Positive and Negative Multiplication, Summation of Products (Positive and Negative), Multiplication (Positive and Negative) and Accumulation, and finally, Division; it should have an automatic floating point arithmetic and an automatic display system.

5.2 THE DIFFERENT REGISTERS NEEDED:-

In order to carry out the various operations listed in the previous Section, the following four registers will be required:

1. SETTING REGISTER (S.R.) - 10 digits capacity
2. PRODUCT REGISTER (P.R.) - 10 digits capacity
3. MULTIPLIER SETTING REGISTER (M.S.R.) - 6 digits capacity
4. STORAGE REGISTER (ST.R.) - 10 digits capacity

5.3 SEQUENCE OF INDEXING AND OUTLINE OF CORRESPONDING MACHINE FUNCTIONS FOR DIFFERENT OPERATIONS:-

A. MIXED ADDITION AND SUBTRACTION:

Ex. 79.3 + 8.879 - 98.21

1. PRESS "CLEAR ALL" - The entire machine is brought to the "ground", i.e., starting state and the display system is turned on.

2. INDEX 7943 - 79.3 is entered into S.R. - S.R. is displayed as 000000079.3.

3. PRESS "+" - The content of S.R. (i.e., 79.3) is added to the content of P.R. (i.e., 0) - S.R. is cleared - P.R., containing (0 + 79.3) i.e., 79.3, is displayed as 000000079.3.

4. INDEX 8.879 - 8.879 is entered into S.R. - S.R. is displayed as 0000008.879.

5. PRESS "+" - The content of S.R. (i.e., 8.879) is added to the content of P.R. (i.e., 79.3) - S.R. is cleared - P.R., containing (79.3 + 8.879) i.e., 88.179, is displayed as 0000088.179.

6. INDEX 98.21 - 98.21 is entered into S.R. - S.R. is displayed as 00000098.21.

7. PRESS "-" - The content of S.R. (i.e., 98.21) is subtracted from the content of P.R. (i.e., 88.179) - S.R. is cleared - P.R., containing (88.179 - 98.21) which is a negative number, is displayed in the complement form, i.e., 9999989.969. The complement form is indicated by an amber lamp.
In order to get the result in the normal form, i.e. -

10.031, an additional key has to be pressed.

8. PRESS "RESTORE" - The content of P.R. (i.e., 9999989.969) is read into S.R. - P.R. is cleared - the content of S.R. (i.e., 9999989.969) is subtracted from the content of P.R. (i.e., 0000000000) - S.R. is cleared - P.R., containing the result in the normal form, is displayed as 0000010.031 with a negative sign.

B. MULTIPLICATION:

Ex. 5.78 x 81.9 =

CASE (i): POSITIVE MULTIPLICATION -

1. PRESS "CLEAR ALL" - Corresponding functions have already been explained.
2. INDEX 5.78 - 5.78 is entered into S.R. - S.R. is displayed as 00000005.78.
3. PRESS "x" - 5.78 is retained undisturbed in S.R. and displayed - M.S.R. is made ready to accept the next entry.
4. INDEX 81.9 - 81.9 is entered into M.S.R. - M.S.R. is displayed as 00081.9.
5. PRESS "=+" - The positive multiplication takes place and the product is added to the content of P.R. - S.R. and M.S.R. are cleared - P.R. is displayed as 0000471.382. Also, input to the M.S.R. is blocked and S.R. is made ready to take in the next number entry.

CASE (ii): NEGATIVE MULTIPLICATION -

Negative multiplication is, in principle, similar to

positive multiplication; however, there will be some changes in the sequence of indexing after step 4 in CASE (i), viz.

5. PRESS "=-" - The negative multiplication takes place and the product is subtracted from the content of P.R. - S.R. and M.S.R. are cleared - P.R. is displayed in the complement form as 9999528.618. The complement form is indicated by an amber lamp.

Also, input to the M.S.R. is blocked and S.R. is made ready to take in the next number entry.

In order to get the result in the normal form, i.e., -0000,471.382, the "RESTORE" key has to be pressed, the functions of which have already been explained under A (i.e., MIXED ADDITION AND SUBTRACTION).

C. <u>SUMMATION OF PRODUCTS (ONLY THE SUM, NOT TOGETHER WITH INDIVIDUAL PRODUCTS, IS REQUIRED)</u>:

Ex. $\underbrace{5.78 \times 81.9}_{P_1} + \underbrace{8.91 \times 7}_{P_2} - \underbrace{151.2 \times 9.759}_{P_3}$

1. PRESS "CLEAR ALL"
2. INDEX 5.78
3. PRESS "X"
4. INDEX 81.9
5. PRESS "=+"

} Corresponding functions have already been explained.

(At this stage P.R., storing $0 + P_1$, is displayed - S.R. and M.S.R. are clear and S.R. made ready to accept the next entry).

6. INDEX 8.91

7. PRESS "X"

8. INDEX 7

9. PRESS "=+"

(P.R. now stores $0+P_1+P_2$ and is displayed - S.R. and M.S.R. are clear and S.R. made ready to accept the next entry).

10. INDEX 151.2

11. PRESS "X"

12. INDEX 9.759

13. PRESS "=-"

(P.R. at this stage, stores $0+P_1+P_2-P_3$ and is displayed - as usual, S.R. and M.S.R. are clear and S.R. made ready to accept the next entry).

Since $0+P_1+P_2-P_3$ is negative, it is displayed in the complement form; this is indicated by an amber lamp.

14. PRESS "RESTORE" - Its purpose and corresponding machine functions have already been explained.

D. <u>MULTIPLICATION AND ACCUMULATION (EACH INDIVIDUAL PRODUCT AS WELL AS THE SUM ARE NEEDED - USEFUL FOR INVOICING)</u>:

Ex. $+ \quad 5.78 \times 81.9 = P_1$

$+ \quad 8.91 \times 7 = P_2$

$- \quad 151.2 \times 9.759 = P_3$

$\text{SUM} = P_1 + P_2 - P_3$

1. PRESS "CLEAR ALL" - Corresponding functions have already been explained.

2. SWITCH ON THE "PRODUCT ACCUMULATOR" - This modifier functions

corresponding to a few keys.

3. INDEX 5.78 - 5.78 is entered into S.R. - S.R. is displayed.
4. PRESS "X" - 5.78 is retained undisturbed in S.R. and displayed - M.S.R. is made ready to accept the next entry - P.R. is cleared.
5. INDEX 81.9 - 81.9 is entered into M.S.R. - M.S.R. is displayed.
6. PRESS "=+" - The first multiplication takes place and the product P_1 is stored in P.R. - S.R. and M.S.R. are cleared - S.R. reads in P_1 from P.R. and P_1 is added from the S.R. to the content of ST.R. (i.e. 0) - S.R. is cleared - P.R., storing P_1, is displayed, while ST.R. accumulates the sum $(0 + P_1)$. Also S.R. is made ready to take in the next entry.
7. INDEX 8.91 - 8.91 is entered into S.R. - S.R. is displayed.
8. PRESS "X" - 8.91 is retained undisturbed in S.R. and displayed - M.S.R. is made ready to accept the next entry - P.R. is cleared.
9. INDEX 7 - 7 is entered into M.S.R. - M.S.R. is displayed.
10. PRESS "=+" - The second multiplication takes place and the product P_2 is stored in P.R. - S.R. and M.S.R. are cleared - S.R. reads in P_2 from P.R. and P_2 is added from S.R. to the content of ST.R. (i.e., $0 + P_1$) - S.R. is cleared - P.R., storing P_2, is displayed, while ST.R. accumulates the sum $(0 + P_1 + P_2)$. Also S.R. is made ready to take in the next entry.

11. INDEX 151.2
12. PRESS "X"
13. INDEX 9.759

} Corresponding functions have already been explained.

14. PRESS "=-" - The third multiplication takes place and the product P_3, in complement form, is stored in P.R. - S.R. and M.S.R. are cleared - S.R. reads in P_3 from P.R. and P_3 is added (not subtracted) from S.R. to content of ST.R. (i.e., $0 + P_1 + P_2$) - S.R. is cleared - P.R., storing the product in the complement form, is displayed while ST.R. accumulates $(0+P_1 + P_2 - P_3)$. Also S.R. is made ready to take in the next entry.

[N.B. - The following illustrative examples will establish the validity of step 14.

Ex. (i):- $8 \times 5 + 2 \times 9 - 2 \times 5$ $\quad [P_3 < P_1 + P_2]$

$P_1 \quad P_2 \quad P_3$

Tracing the 14 steps described so far, one finds that after step 10, the contents of P.R. and ST.R. are

P.R. : 18 (i.e., P_2) ST.R. : 58 (i.e., $P_1 + P_2$)

or 0000000018 or, 0000000040 P_1

$+$ 0000000018 P_2

0000000058 $P_1 + P_2$

After step 14 :

P.R. : -10 (i.e., P_3) ST.R. : 48 (i.e., $P_1 + P_2 - P_3$)

or 9999999990 or, 0000000058 $P_1 + P_2$

$+$ 9999999990 P_3

$\uparrow$ 0000000048 $P_1 + P_2 - P_3$

In this example final result was positive; however, it is negative in the next example.

Ex. (ii): $8 \times 5 + 2 \times 9 - 6 \times 12$

$P_1 \quad P_2 \quad P_3$

After step 10:

Same as in the previous example.

After step 14:

P.R. : -72 (i.e., P_3) ST.R. : -14 (i.e., $P_1+P_2-P_3$)

or, 9999999928 or, 0000000058 $P_1 + P_2$

$+$ 9999999928 P_3

9999999986 $P_1+P_2-P_3$

Thus, in this example, the final result is negative and is stored in ST.R . in the complement form.]

Now, since the P.R. stores and displays a negative product in the complement form, (indicated by the amber lamp), it has to be restored to the normal form by pressing the "RESTORE" key as usual.

15. PRESS "RESTORE" - The corresponding functions have been described previously.

16. PRESS "SUM" - The content of ST.R., i.e., $(0 + P_1 + P_2 - P_3)$ is read into S.R. (directly, if positive and after automatic restoration, if negative) - S.R., storing the final result in the normal form, is displayed.

Automatic restoration of the content of ST.R. :

For this, once it is detected that the content is in complement form, the usual restoring technique is applied. Since

S.R. was cleared in Step 15, the content of ST.R. in complement form is read into S.R. and ST.R. is cleared. The content of S.R. is then subtracted from that of ST.R. (i.e., 0) and S.R. is cleared.

E. DIVISION:

Ex. 859.7 ÷ 3.79 =

1. PRESS "CLEAR ALL"
2. INDEX 859.7 - 859.7 is entered into S.R. - S.R. is displayed as 000000859.7.
3. PRESS "÷" - 859.7 is added from S.R. to the content of P.R. (i.e., 0) - S.R. is cleared - P.R. is displayed as 000000859.7.
4. INDEX 3.79 - 3.79 is entered into S.R. - S.R. is displayed as 00000003.79.
5. PRESS "÷" - Division takes place and the quotient is stored in M.S.R. - P.R. and S.R. are cleared - M.S.R. is displayed as 226.833.

5.4 LIST OF THE DIFFERENT KEYS, SWITCHES, INDICATORS, ETC. TO BE FOUND ON THE CONSOLE:-

SERIAL NO.	DESCRIPTION	NO. OF PIECES
1.	ON/OFF SWITCH	1
2.	CLEAR ALL KEY	1
3.	CLEAR S.R. KEY	1
4.	CLEAR M.S.R. KEY	1
5.	NUMERALS KEYS	10

SERIAL NO.	DESCRIPTION	NO. OF PIECES
6.	DECIMAL POINT KEY	1
7.	+, −, x, ÷ KEYS	4
8.	=+, =−, ÷ KEYS	3
9.	PRODUCT ACCUMULATOR ON/OFF SWITCH	1
10.	RESTORE KEY	1
11.	SUM KEY	1
12.	NIXIE TUBES - NUMERIC	10
	NIXIE TUBE - SIGN	1
13.	NEON LAMP FOR INDICATING DECIMAL POINT	11
14.	COMPLEMENT FORM INDICATING AMBER LAMP	1
15.	OVERFLOW INDICATING RED LAMP	1
16.	'POWER ON' INDICATING NEON LAMP	1

5.5 MODIFICATIONS IN THE DISPLAY UNIT:-

Although possibly obvious, the few modifications required to be introduced in the display unit of the present machine are being listed below for completeness.

(i) The display unit will have a 10-digits capacity instead of 5-digits.

(ii) Four registers will have to be displayed, because of the introduction of one extra register, viz., STORAGE REGISTER.

(iii) Since M.S.R. has a capacity of 6 digits only, the first four NIXIE TUBES from the left will remain dark when M.S.R. is displayed.

(iv) The decimal point will be displayed by the glow of any one of the 11 neon lamps placed in between the ten NIXIE

TUBES (9 in this manner) and at the two ends (2 in this manner)
Fig. 5.1)

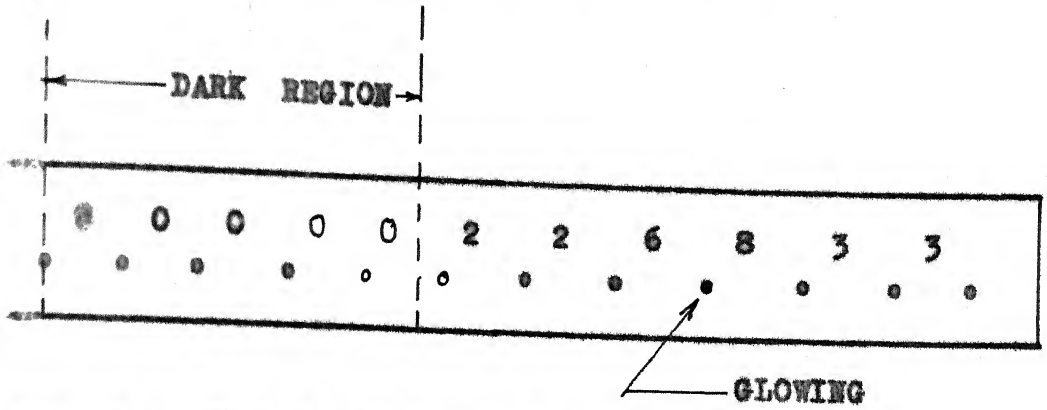


FIG. 5.1 OPERATOR'S VIEW OF M.S.R. DISPLAY

(Reads 226.883)

(v) Blanking: When the display is blanked, the numerals as well as the decimal point are blanked.

CHAPTER - VI

6.1 FLOATING POINT ARITHMETIC:-

Since counter type arithmetic is being used, all the operations in the floating point mode will necessarily be executed in the integer mode but the decimal point has to be properly taken care of simultaneously by some additional floating point arithmetic which is also proposed to be counter type. The principle of carrying out floating point arithmetic can be broadly stated as follows:

A. ADDITION/SUBTRACTION - Before the start of the operation, the two operands must be lined-up properly with respect to the decimal point.

B. MULTIPLICATION - The multiplication is performed in the integral mode and afterwards the decimal point is supplied. The number of digits after decimal in the product equals the sum of the number of digits after decimal in the multiplicand and that in the multiplier.

C. MULTIPLICATION AND ACCUMULATION - Before carrying out a multiplication, the anticipated product and the sum of the products already accumulated should be lined up with respect to the decimal point; only after this the multiplication and subsequent accumulation can be executed.

D. DIVISION - Since division is carried out by repeated

subtraction, the dividend and the divisor should first be lined up with respect to the decimal point and then the process of division will start with digit-equalling, as was explained in Section 4.2.4.

The method of achieving floating point arithmetic has been explained below, along with corresponding keying sequence, for the various operations.

6.2 METHOD OF ACHIEVING AUTOMATIC DECIMAL POINT ADJUSTMENT:-

6.2.1. MIXED ADDITION AND SUBTRACTION:

Ex. 529.238 + 39.3 -2 + .85962 - 30.7 =

a) For carrying out the process of mixed addition and subtraction with floating point arithmetic, the following three counters will be needed:

i) AUGEND COUNTER - A Decade UP counter
ii) ADJUSTMENT COUNTER - " UP-DOWN counter
iii) ADDEND COUNTER - " UP counter

a) During the indexing of operands, one pulse per each digit after the decimal point is input to each of the above-mentioned counters, which may be enabled or disabled and counting up or down, depending on the particular operation or a particular sequence in the same operation. However, this is applicable to all the operations going to be described subsequently.

Now, it will be worthwhile to keep track of the behaviour of the counters along with the sequence of indexing.

1. PRESS "CLEAR ALL" - (i) All the three counters are cleared. (ii) The AUGEND counter is enabled, the ADDEND counter is

disabled and the ADJUSTMENT counter is set to count up (after being enabled). (iii) The decimal point of the display unit, which is connected to S.R., is set to be read from the AUGEND counter.

NOTE:- While all the registers will store numbers in the integer mode, only the content of the register being displayed will be furnished with the decimal point (to be read from the appropriate counter). A diagram outlining the method of decimal point display has been provided in Fig. 6.1.

2. INDEX 529.238 - (i) The number 529238 is stored in S.R. (without any decimal point). (ii) At the end of the indexing operation, the three counters will read

AUGEND - 3 ; ADJUSTMENT - 3 ; ADDEND - 0 ;

(iii) So, the S.R. is displayed as 0000529.238.

3. PRESS "+" - (i) The AUGEND counter is disabled, the ADDEND counter is enabled and the ADJUSTMENT counter is made ready to count down. (ii) The content of S.R., i.e., 0000529238, is added to that of P.R., i.e., 0000000000, and S.R. is subsequently cleared.

(iii) The P.R., being displayed, reads 0000529.238 (since the decimal point is still set from the AUGEND counter).

4. INDEX 39.3 - (i) The number 393 is entered into S.R. (ii) As soon as the first digit, i.e., 3 is entered, the display unit is connected back to S.R. and its decimal point is set from the ADDEND counter. (iii) At the completion of indexing, the counter readings are

AUGEND - 3 ; ADJUSTMENT - 2 ; ADDEND - 1 ;

(Incidentally, there was no borrow from the ADJUSTMENT counter as the addend has less number of digits after decimal than the ~~AUGEND~~ augend).

(iv) The S.R., being displayed, reads 000000039.3.

5. PRESS "+" - This is the second occasion of using the "+" (or "-") key and this, together with all the successive "+" (or "-") keyings, should be distinguished from the first as the former have to perform some extra functions compared to the latter.

(i) Lining-up: As there was no borrow from the ADJUSTMENT counter during step 4 and the ADJUSTMENT counter reading is non-zero, the S.R. storing 0000000393, is shifted left and one pulse per each shifting is entered into the ADJUSTMENT counter (counting down) as well as the ADDEND counter (counting up). The shifting stops when the ADJUSTMENT counter reads zero, so that only two shiftings are needed. Thus, at the completion of the process of lining up, the S.R. stores 0000039300 while the P.R. stores 0000529238; the counter readings are:

AUGEND - 3 ; ADJUSTMENT - 0 ; ADDEND - 3.

(ii) The decimal point of the display is connected to the AUGEND counter.

(iii) The addition takes place and the sum 0000568538, stored in P.R., is displayed as 0000568.538.

(iv) Preparations for the next operand: The ADJUSTMENT counter reads in the content of the AUGEND counter (it is set to count down) while the ADDEND counter is reset. (The AUGEND and the ADDEND counter remain disabled and enabled respectively.) The

counter readings, at this stage, are:

AUGEND - 3; ADJUSTMENT - 3; ADDEND - 0.

6. INDEX 2 - Functions performed are the same as explained under step 4. The counter readings remain unchanged, i.e.,

AUGEND - 3; ADJUSTMENT - 3; ADDEND - 0;

The S.R. is displayed as 0000000002.

7. PRESS "-" - (i) Lining up: Since there was no borrow from the ADJUSTMENT counter in step 6 and its reading is non-zero, the lining up is achieved in exactly the same way as described under step 5(i). So, at the completion of the process of lining up, the S.R. stores 0000002000 while the P.R. stores 0000568538 and the different counter readings are:

AUGEND - 3; ADJUSTMENT - 0; ADDEND - 3;

(ii) Same as in step 5(ii).

(iii) The subtraction takes place and the difference 0000566538, stored in P.R., is displayed as 0000566.538.

(iv) Preparations for the next operand: Same as explained in step 5(iv). The counter readings become:

AUGEND - 3; ADJUSTMENT - 3; ADDEND - 0;

8. INDEX .85962 - The counter readings become:

AUGEND - 3; ADJUSTMENT - 8 (plus a borrow); ADDEND - 5

The S.R., being displayed, reads 00000.85962.

9. PRESS "+" - (i) Lining-up: (a) As a borrow was obtained from the ADJUSTMENT counter during step 8, the AUGEND counter is enabled, the ADDEND counter is disabled and the ADJUSTMENT counter is made ready to count up.

(b) Since the ADJUSTMENT counter reading is non-zero, the P.R.,

storing 0000566538, is shifted left and one pulse per each shifting is entered into the ADJUSTMENT counter (counting up) and the AUGEND counter (counting up). The shifting stops as soon as the ADJUSTMENT counter reads zero. Thus, at the completion of the process of lining up, the S.R. stores 0000085962 while the P.R. stores 0056653800 and the various counter readings become:

AUGEND - 5; ADJUSTMENT - 0; ADDEND - 5;

(ii) Same as in step 5(ii).

(iii) The addition takes place and the sum 0056739762, stored in P.R., is displayed as 00567.39762.

(iv) Preparations for the next operand: In addition to what have been listed under step 5(iv), the AUGEND counter is disabled, the ADDEND counter is enabled and the ADJUSTMENT counter is set to count down. This was necessitated by step 9(i)(a) . The different counter readings, at this stage, are:

AUGEND - 5; ADJUSTMENT - 5; ADDEND - 0;

10. INDEX 30.7 - The counter readings become:

AUGEND - 5; ADJUSTMENT - 4; ADDEND - 1.

The S.R. is displayed as 000000030.7.

11. PRESS "-" - (i) Lining-up: Since there was no borrow from the ADJUSTMENT counter in the previous step, the procedure for lining up will be same as in step 5(i). The S.R. and P.R. store 0003070000 and 0056739762 respectively; the different counter readings are:

ADDEND - 5; ADJUSTMENT - 0; ADDEND - 5;

(ii) Same as in step 5(ii).

(iii) The subtraction takes place and the difference (in fact the final result) 0053669762, stored in P.R., is displayed as 00536.69762.

(iv) Preparations for the next operand: Same as explained in step 5(iv). The counter readings become:

AUGEND - 5; ADJUSTMENT - 5; ADDEND - 0;

6.2.2 MULTIPLICATION:-

Ex. 753.095 x 83.71 =

In addition to the three counters, viz. AUGEND, ADJUSTMENT and ADDEND, one more counter, viz.

iv) STORAGE COUNTER - A Decade Up counter, is required for floating point multiplication, explained below with the indexing sequence.

1. PRESS "CLEAR ALL" - Already explained in Section 6.2.1. In addition, the STORAGE counter is disabled.

2. INDEX 753.095 - Same as explained in Section 6.2.1. (step 2). At the end of the indexing operation, readings of the different counters are:

AUGEND - 3; ADJUSTMENT - 3; ADDEND - 0; STORAGE - 0;

S.R., storing 0000753095, is displayed as 0000753.095.

3. PRESS "x" - This disables the AUGEND counter and enables the ADDEND counter. (The ADJUSTMENT counter continues to count up).

4. INDEX 83.71 - (i) The number 8371 is entered into M.S.R. (ii) As soon as the first digit, i.e., 8 is entered, the display unit is connected to M.S.R. and its decimal point is set from the

ADDEND counter. (iii) At the completion of indexing, the counter readings are:

AUGEND - 3; ADJUSTMENT - 5; ADDEND - 2; STORAGE - 0;

(iv) The M.S.R., storing 008371 is displayed as 0083.71.

5. PRESS "=+" (or =-) - (i) For the next operand, the AUGEND counter is enabled while the ADDEND counter is disabled.

(ii) The STORAGE counter reads-in the content of the ADJUSTMENT counter and the decimal point of the display, which is, incidentally, connected to P.R., is set to be read from the STORAGE counter. The counter readings become:

AUGEND -3; ADJUSTMENT - 5; ADDEND - 2; STORAGE - 5;

(iii) The multiplication takes place and the product, stored in P.R., is displayed as 63041.58245.

(iv) After the multiplication, both the AUGEND and the ADDEND counters are cleared and the ADJUSTMENT counter is ~~made~~ set to count down. Thus at the end, the readings of the four counters become:

AUGEND - 0; ADJUSTMENT - 5; ADDEND - 0; STORAGE -5;

6.2.3 <u>SUMMATION OF PRODUCTS</u>:-

Ex. 753.095 x 83.71 + 12 x .856 + 17.9513 x 8.71
+ .8975612 x 14.

1. PRESS "CLEAR ALL"
2. INDEX 753.095.
3. PRESS "x"
4. INDEX 83.71
5. PRESS "=+"

The behaviour of the different counters, upto this step (step 5), have been described in the preceding Section

(Section 6.2.2). The counter readings, at the end of step 5, are:

AUGEND - 0; ADJUSTMENT - 5; ADDEND - 0; STORAGE - 5;

6. INDEX 12 - (i) The number 12 is entered into S.R.

(ii) As soon as the first digit, i.e., 1, is entered, the display unit is connected to S.R. and its decimal point is set from the AUGEND counter.

(iii) At the end of the indexing operation, the counter readings are:

AUGEND - 0; ADJUSTMENT - 5; ADDEND - 0; STORAGE - 5;

(iv) The S.R., storing 0000000012, is displayed as 0000000012.

7. PRESS "x" - Same as explained in step 3.

8. INDEX .856 - Same as in step 4. The counter readings become:

AUGEND - 0; ADJUSTMENT - 2; ADDEND - 3; STORAGE - 5;

M.S.R., storing 000856, is displayed as 000.856.

Incidentally, there was no borrow from the ADJUSTMENT counter.

9. PRESS "=+" - (i) Same as (i) in step 5.

(ii) Since there was no borrow from the ADJUSTMENT counter in step 8 and its reading is non-zero, the S.R. is shifted left and one pulse per each shifting is entered into the ADJUSTMENT counter (counting down) and the AUGEND counter (counting up). Two shiftings are needed to make the ADJUSTMENT counter read zero and the different counter readings become:

AUGEND - 2; ADJUSTMENT - 0; ADDEND - 3; STORAGE - 5;

Now, the S.R. stores 0000001200.

(iii) The lining-up being complete, the multiplication takes

place and this second product is accumulated in the P.R. The decimal point of the display unit, connected to P.R., is set from the STORAGE counter, which reads 5.

(iv) The AUGEND and the ADDEND counter are cleared while the ADJUSTMENT counter is made to read-in the content of the STORAGE counter so that the final counter readings become:

AUGEND - 0; ADJUSTMENT - 5; ADDEND - 0; STORAGE - 5;

NOTE: This second =+ (or =-) and the successive ones have to be distinguished from the first =+ (or =-) command.

10. INDEX 17.9513 - Same as in step 6. The readings of the different counters are:

AUGEND - 4; ADJUSTMENT - 1; ADDEND - 0; STORAGE - 5.

11. PRESS "x" - Already explained.

12. INDEX 8.71 - Same as in step 8. The various counters now read:

AUGEND - 4; ADJUSTMENT - 9; ADDEND - 2; STORAGE - 5;

13. PRESS "=+" - (i) Same as in step 9.

(ii) Since a borrow was obtained, the ADJUSTMENT counter is set to count up and the STORAGE counter is enabled to count up.

(iii) The ADJUSTMENT counter reading being non-zero, P.R. is shifted left and one pulse per each shifting is entered into the ADJUSTMENT and the STORAGE counter. After one shifting, the ADJUSTMENT counter reading is brought back to zero and the different counter readings become:

AUGEND - 4; ADJUSTMENT - 0; ADDEND - 2; STORAGE - 6;

(iv) Same as (iii) in step 9.

(v) Same as (iv) in step 9. The various counter readings are:

AUGEND - 0; ADJUSTMENT - 6; ADDEND - 0; STORAGE - 6;

(vi) As a follow up action of (ii), the ADJUSTMENT counter is set to count down and the STORAGE counter is disabled.

14. INDEX .8975692 - The various counter readings now become:

AUGEND - 7; ADJUSTMENT - 9; ADDEND - 0; STORAGE - 6;

15. PRESS "x" - Already explained.

16. INDEX 14 - The counter readings remain unchanged, viz.

AUGEND - 7; ADJUSTMENT - 9; ADDEND - 0; STORAGE - 6;

17. PRESS "=+" - The functions in this case are identical to those listed in step 13. At the end of (iii), the various counter readings are:

AUGEND - 7; ADJUSTMENT - 0; ADDEND - 0; STORAGE - 7;

and in (v), the counter readings become:

AUGEND - 0; ADJUSTMENT - 7; ADDEND - 0; STORAGE - 7;

6.2.4 MULTIPLICATION AND ACCUMULATION - INVOICING:-

The method of achieving floating point arithmetic in this case is essentially the same as explained under the preceding Section (Section 6.2.3), the only modification being that with the pressing of the second or successive =+ (or =-) keys, ST.R., instead of P.R., is shifted (if a borrow was obtained in the preceding step).

6.2.5 DIVISION:-

For the purpose of carrying out floating point division, the following counters are required:

A.	AUGEND	Decade up	counter
B.	ADJUSTMENT	" up-down	"
C.	AUGEND	" up	"
D.	DIGITS	" up-down	"
E.	QUOTIENT	Count-of-six down	"
F.	CHECK	Decade up	"

The principle of operation together with the use of the six counters will be illustrated with two examples, one with a quotient greater than unity and the other with a quotient less than unity - as these two cases call for slightly different procedures.

Ex. 1: 1579.3 ÷ 29.753 = 053.080.

1. PRESS "CLEAR ALL" - All the six counters are cleared. The AUGEND counter is enabled, the ADDEND counter is disabled and the ADJUSTMENT as well as the DIGITS counter are set to count up. The QUOTIENT counter together with the CHECK counter is disabled.

The decimal point of the display, which is connected to S.R., is set from the AUGEND counter reading.

2. INDEX 1579.3 - After the indexing the various counters read: AUGEND-1; ADJUSTMENT-1; ADDEND-0; DIGITS-5; QUOTIENT-0; CHECK-0; S.R., storing 0000015793, is displayed as 000001579.3.

3. PRESS "÷" - The AUGEND counter is disabled, the ADDEND counter is enabled and the ADJUSTMENT as well as the DIGITS counter are set to count down. The decimal point of the display remains connected to the AUGEND counter.

The content of S.R. is added to the content (i.e., 0) of P.R. S.R. is cleared and P.R., storing 0000015793, is displayed

as 000001579.3.

4. INDEX 29.753 - The counter readings become

AUGEND-1; ADJUSTMENT-8; ADDEND-3; DIGITS-0; QUOTIENT-0; CHECK-0;

As soon as the first digit, i.e., 2 was entered, the display unit and its decimal point were connected to S.R. and the ADDEND counter respectively, so that now S.R., storing 0000029753, is displayed as 0000029.753.

5. PRESS "÷" - (i) It is checked whether the divisor, stored in S.R., is zero. If it is zero, then the process of division is not carried out at all and the overflow indicating red lamp is lighted. However, if it is non-zero, then

(ii) The QUOTIENT counter is set to count down.

(iii) The two operands have to be lined up with respect to the decimal point by the same method as was described in Section 6.2.1 (step 9)*. At the end of the lining up operation, a pulse is entered into the QUOTIENT counter, so that the different counter readings become:

AUGEND-3; ADJUSTMENT-0; ADDEND-3; DIGITS-2; QUOTIENT-6; CHECK-0;

Now, the S.R. and P.R. read 0000029753 and 0001579300 respectively.

*A pulse per each shifting is also entered into the DIGITS counter (counting up when P.R. is shifted and counting down when S.R. is shifted), for obvious reasons.

(iv) Since the DIGITS counter reading is "positive" (i.e., the DIGITS counter has no standing borrow) as well as non-zero, the next step will be "digit equalling". After the digit-equalling, the method which was described in Section 4.3.4 under PRESS "÷", the counter readings become:

AUGEND-3; ADJUSTMENT-0; ADDEND-3; DIGITS-0; QUOTIENT-6; CHECK-2;

So, the S.R. reads 0002975300 and P.R. reads 0001579300.

(v) The CHECK counter is enabled to count down.

(vi) The content of S.R. is now subtracted repeatedly from that of P.R. and for each subtraction (except when a borrow is obtained), a pulse is entered into the M.S.R. which is counting up; the process (already explained in Section 4.2.4) is illustrated below for the present example.

		M.S.R. READING	CHECK COUNTER READING	QUOTIENT COUNTER READING
P.R. :	0001579300	000000	2	6
S.R. :	0002975300			
	−			
	↓ 9998604000			

Since with the last subtraction a borrow was obtained,

(a) no pulse is entered into M.S.R. and instead, a pulse is entered into the QUOTIENT counter (counting down) and the content of S.R. is added once to the content of P.R., i.e.

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	9998604000	000000	2	6
S.R. :	0002975300			
	+			
	↑ 0001579300	000000	2	5

At the end of step (a), i.e., restoration, the reading of the CHECK counter is tested for zero. Since it was a zero,

(b) the S.R. is shifted right by one place, the M.S.R. is shifted left by one place, a pulse is entered into the CHECK counter (counting down) and the process of repeated subtraction is started again.

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0001579300	000000	1	5
S.R. :	0000297530			
	0001281770	000001	1	5

This repeated subtraction is continued 5 times uninterrupted. So, during the sixth subtraction

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000091650	000005	1	5
S.R. :	0000297530			5
	↓ 9999794120	000005	1	5

Since a borrow is obtained, step (a) is repeated so that the various readings become:

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000091650	000005	1	4

Now that the CHECK counter reading is non-zero, the step (b) is repeated and hence

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000091650	000005	0	4
S.R. :	0000029753			
	0000061897	000051	0	4

This is repeated 2 more times uninterrupted and after that the readings of the various counters are:

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000002391	000053	0	4
S.R. :	0000029753			
	↓ 9999972638	000053	0	4

Since a borrow is obtained, step (a) is again repeated, so that the various readings become:

	M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000002391	000053	0 3

Now, because the CHECK counter reading is zero, step (b) is not repeated and instead

(vii) The DIGITS counter is reset and the content of the QUOTIENT counter (i.e., 3) is jam transferred into it. The decimal point of the display unit, which is connected to M.S.R., will be set from the DIGITS counter.

(viii) The QUOTIENT counter reading is tested for zero. Since it is found to be non-zero, (c) the P.R. and M.S.R. are shifted one place to the left and the process of repeated subtraction is resumed.

	M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000023910	000530	0 3
S.R. :	0000029753		
	9999994157	000530	0 3

Since a borrow is obtained, step (a) is repeated, so that the counter readings become:

	M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000023910	000530	0 2

Now the QUOTIENT counter reading is tested for zero and as it is non-zero, step (c) is repeated so that

	M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000239100	005300	0 2
S.R. :	0000029753		
	0000209347	005301	0 2

This is repeated 7 times without interruption and after that

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000001076	005308	0	2
	0000029753			
	-			
	↓ 9999971323	005308	0	2

Since a borrow is obtained, step (a) is repeated and the various readings become:

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000001076	005308	0	1

Now that the QUOTIENT counter reading is not zero, step (c) is repeated. So

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000010760	053080	0	1
	0000029753			
	-			
	↓ 9999981007	053080		1

Since a borrow is obtained, step (a) is repeated, so that the various readings are:

		M.S.R.	CHECK COUNTER	QUOTIENT COUNTER
P.R. :	0000010760	053080	0	0

Now, the QUOTIENT counter reading is zero and hence the operation of division is deemed to have been completed. So, M.S.R., storing 053080, is displayed as 053.080 [See (vii)].

NOTE: Since the capacity of the M.S.R. is only 6 digits, care should be taken to see that the operands are never such that the integer portion of the quotient may exceed 6 digits; because, in

6.3 ABOUT THE DIFFERENT REGISTERS AND COUNTERS TO BE USED:-

The configuration, features and functions of the different registers and counters to be used in this "more sophisticated machine" are almost identical to that explained in Section 4.1, excepting for a few changes, which have been mentioned below together with the description of the additional registers and counters.

6.3.1 MODIFICATIONS TO BE INTRODUCED OVER THE DESCRIPTION PROVIDED IN SECTION 4.1:-

1. S.R. - S.R. is of 10-digit capacity and can read-in the content of P.R. as well as ST.R.
2. P.R. - P.R. is of 10-digit capacity and consequently is provided with 10 individual input gates for the 10 decade counters.
3. M.S.R. - It is of 6-digit capacity.
4. COUNTER 1 - No change.
5. COUNTER 2 - It is a DECADE UP COUNTER and its reading determines the place of entry of pulses corresponding to a digit (in S.R.) into both P.R. as well as ST.R.
6. COUNTER 3 - No change.
7. COUNTER 4 - This is a COUNT-OF-6 UP COUNTER.
8. DIGITS COUNTER - It is a DECADE UP-DOWN COUNTER.
9. CHECK COUNTER - It is a DECADE DOWN COUNTER.

6.3.2 ADDITIONAL REGISTERS AND COUNTERS:-

9. STORAGE REGISTER (ST.R.) - This is just a duplicate of the P.R.

10. AUGEND COUNTER
11. ADJUSTMENT COUNTER
12. ADDEND COUNTER
13. STORAGE COUNTER
15. QUOTIENT COUNTER

All of these have already been described at the appropriate points in Section 6.2.

6.4 DISPLAYING THE DECIMAL POINT:-

From what we have discussed so far about the display system (see Sections 3.4 and 5.5), it is clear that at the different points of the computations, the decimal point is set from the readings of any of the four counters- AUGEND, ADDEND, STORAGE and DIGITS. Fig. 6.1 schematically illustrates the arrangement proposed to be employed for displaying the decimal point and is similar to Fig. 3.4.

6.5 PRINCIPLE OF MACHINE ARITHMETIC:-

It is essentially the same as described in CHAPTER IV (Section 4.2), excepting, however, a few modifications as were brought out in Section 6.2.5, which were required to be introduced for the process of DIVISION.

6.6 DETAILED METHOD OF ACHIEVING THE FLOATING POINT ARITHMETIC (i.e., ACHIEVING THE INTEGER MODE MACHINE ARITHMETIC AND SIMULTANEOUSLY TAKING CARE OF THE DECIMAL POINT):-

The methods of achieving both the integer mode machine arithmetic as well as the automatic decimal point adjustment have already been illustrated independently in Sections 4.2 and 6.2

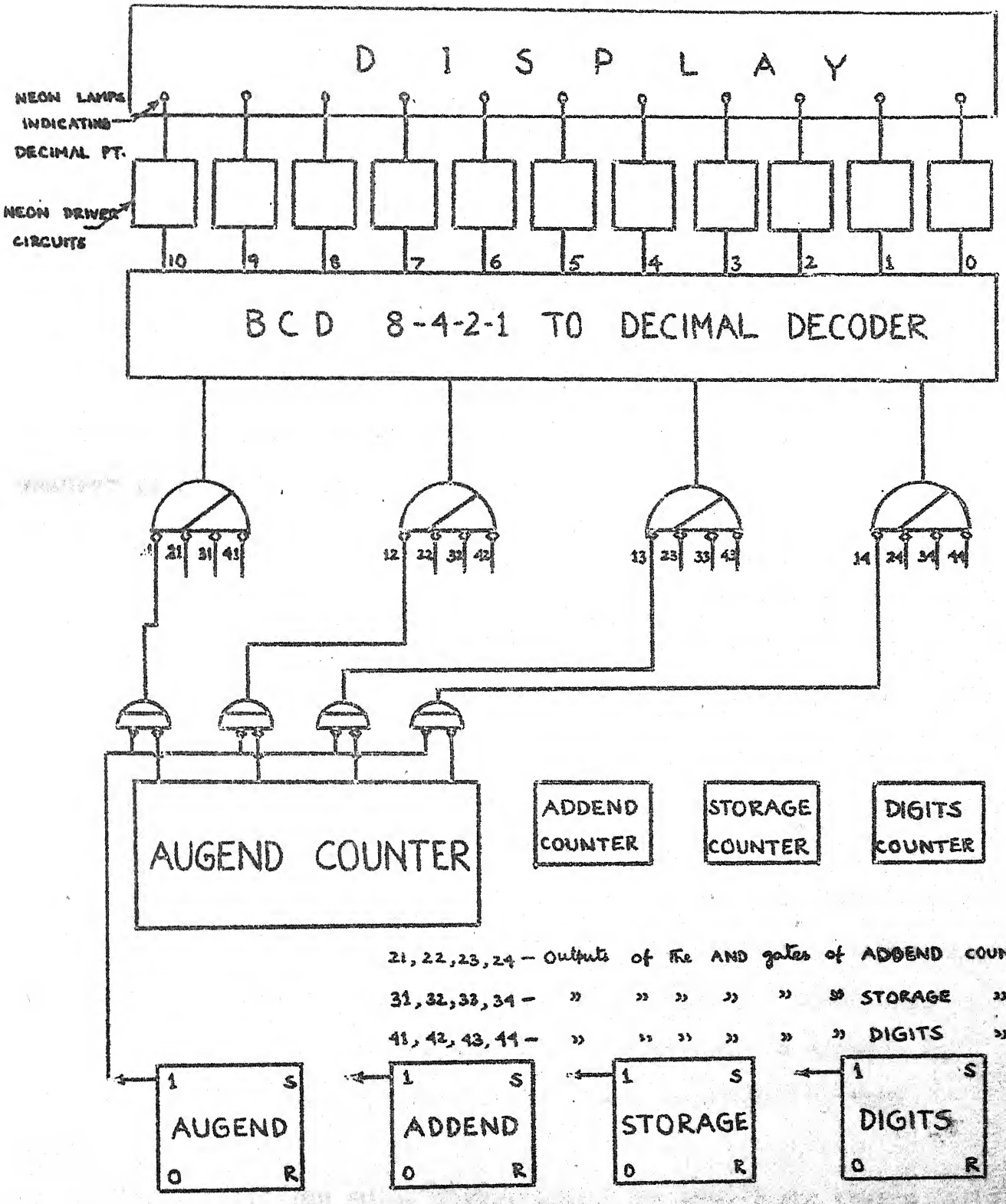


FIG. 6·1 DECIMAL POINT DISPLAY

respectively. These two, when integrated with appropriate time sequence, can form the content of this Section. However, this is not being done presently to avoid unnecessary repetitions and it will find its place, though in somewhat different form, in the following Section.

6.7 DETAILED FUNCTIONS CORRESPONDING TO DIFFERENT KEYS:-

1. "ON-OFF" SWITCH - Switches the power supply ON or OFF.
2. "CLEAR ALL" - (i) All the registers and counters in the machine are cleared and the various flip-flops are returned to their "ground states". The Product Accumulator is turned off if it was ON. (ii) The AUGEND counter is enabled, the ADDEND counter is disabled and the ADJUSTMENT as well as the DIGITS counter are set to count up. (iii) The display unit is connected to S.R. and is blanked. The decimal point of the display is set to be read from the AUGEND counter. (iv) S.R. is made ready to accept the next operand (i.e., the first operand in any of the five operations) and consequently entry into M.S.R. is blocked.
3. "CLEAR S.R." - S.R. is cleared.
4. "CLEAR M.S.R." - M.S.R. is cleared.

NOTE:- Besides clearing the respective registers, the CLEAR S.R. and CLEAR M.S.R. keys may have to perform some associated functions, which can be listed only after studying the effect of these keys on the different counters (as was done for the 5-digit machine in Section 4.3.5). However, this has not been considered in this Thesis.

5. NUMERALS - (i) The pulse corresponding to each digit blanks

the display. (ii) As soon as the digit is entered into it, the S.R. or the M.S.R., as the case may be, is shifted left by one place and immediately after completion of the shifting, blanking on the display is withdrawn. (iii) During indexing of operands (a) each digit pulse is input to the DIGITS counter (which may be enabled or disabled, counting up or down), (b) each digit pulse after the decimal point is input to the AUGEND, ADDEND and ADJUSTMENT counter (which may be enabled or disabled, counting up or down).

(iv) As soon as the first digit of the second or successive operands (including the first operands of the second or successive products during the accumulative multiplications) is entered, the display unit is connected to either S.R. or M.S.R. and its decimal point is set from either the ADDEND or the AUGEND counter, depending on the particular operation or the particular step in the same operation.

6. "DECIMAL" KEY - It enables the digit pulses following it to be input to the AUGEND, ADDEND and ADJUSTMENT counter.

7. "+" - Since the functions corresponding to the first use of the "+" key are different from those corresponding to the second or successive uses, during the operation of MIXED ADDITION AND SUBTRACTION, they will be listed under separate headings.

(I) FIRST "+" - (i) The P.R. is set to count up. (ii) The display is connected to P.R. and is blanked. (iii) The DIGITS counter is disabled and reset. (iv) The AUGEND counter is disabled, the ADDEND counter is enabled and the ADJUSTMENT counter is made ready to count down.

(v) An ADDITION/SUBTRACTION CYCLE (described in Section 4.3.1) is started to add the content of S.R. to the content of P.R. At the end of the cycle, a carry is generated from COUNTER 2, as usual.

(vi) The carry obtained in (v) is used to (a) clear the S.R. and (b) remove the blanking of the display.

(II) SECOND AND SUCCESSIVE "+" -

(i) } Same as the corresponding steps in
(ii) } (I) (i.e., FIRST "+").

(iii) Lining-up: The procedure for lining up the two operands with respect to the decimal point will be different for the two cases, viz. (a) when a borrow has been obtained from the ADJUSTMENT counter during the preceding step of entering the ADDEND, and (b) when no borrow has been obtained.

CASE (A):

If a borrow was obtained,

(a) the AUGEND counter is enabled, the ADDEND counter is disabled and the ADJUSTMENT counter is set to count up.

(b) since the ADJUSTMENT counter reading must be non-zero, the P.R. is shifted left and one pulse per each shifting is entered into the ADJUSTMENT counter (counting up) and the AUGEND counter (counting up). The shifting is discontinued as soon as the ADJUSTMENT counter reads zero.

CASE (B):

If no borrow was obtained,

(a) the ADJUSTMENT counter reading is tested . If it is found to be zero, no lining-up is needed. If, however, it is

non-zero,

(b) the S.R. is shifted left and one pulse per each shifting is entered into the ADJUSTMENT counter (counting down) as well as the ADDEND counter (counting up). The shifting is stopped as soon as the ADJUSTMENT counter reads zero.

(iv) Same as (v) in (I).

(v) Same as (vi) in (I).

(vi) Preparations for the next operand - (a) The ADJUSTMENT counter reads in the content of the AUGEND counter while the ADDEND counter is reset. (b) The AUGEND counter is disabled, the ADDEND counter is enabled and the ADJUSTMENT counter is set to count down.

NOTE:- The action (b), although not needed for CASE (B), is necessary because of step (a) of CASE (A).

8. "-" - Same as that for "+" except that in step (i), the P.R. is set to count down.

9. "x" - (i) M.S.R., instead of S.R., is enabled to accept the next operand.

(ii) The DIGITS counter is disabled and reset.

(iii) The AUGEND counter is disabled while the ADDEND counter is enabled.

(iv) If the PRODUCT ACCUMULATOR is ON, the P.R. is cleared.

10. "÷" - (i) P.R. is set to count up.

(ii) The DIGITS counter, still enabled, is made ready to count down.

(iii) The display is connected to P.R. and is blanked.

(iv)
(v) } Same as the corresponding steps for "+" key
(vi) } CASE (I) i.e., FIRST "+".

11. "=+" - In case of "=+" (or "=-") key, four distinct cases arise which call for different sets and sequences of machine functions. Accordingly, the four cases have been treated separately, as shown below:

<u>CASE I - PRODUCT ACCUMULATOR OFF - FIRST "=+" in course of the operation</u>:

(i) The P.R. is set to count up.

(ii) The AUGEND counter is enabled while the ADDEND counter is disabled (as a preparation for the next operand).

(iii) The display unit is connected to P.R. and is blanked. Its decimal point is set to be read from the STORAGE counter.

(iv) The STORAGE counter reads-in the content of the ADJUSTMENT counter.

(v) A MULTIPLICATION CYCLE (described in Section 4.3.3) is initiated at the end of which a carry is given out by COUNTER 4.

(vi) The carry obtained in the preceding step (a) clears the S.R. and M.S.R., (b) clears both the AUGEND and the ADDEND counter and sets the ADJUSTMENT counter to count down, (c) removes the blanking of the display, and (d) blocks the input to M.S.R., so that S.R. is made ready to take in the next entry.

<u>CASE II - PRODUCT ACCUMULATOR OFF - SECOND AND SUCCESSIVE "=+" in course of the operation</u>:

(i)
(ii) } Same as in CASE I.
(iii)

(iv) Lining-up of this product with the sum of products already accumulated - As in the case of SECOND AND SUCCESSIVE "+" (or "-") keying, in the case of SECOND AND SUCCESSIVE "=+" also, the procedure for lining up will be different for the following two cases:

(A) If a borrow was obtained from the ADJUSTMENT counter during the indexing of the multiplier, then

(a) the ADJUSTMENT counter is set to count up and the STORAGE counter is enabled (to count up).

(b) the ADJUSTMENT counter being non-zero, the P.R. is shifted left and one pulse per each shifting is entered into the ADJUSTMENT counter (counting up) and the STORAGE counter (counting up). The shifting stops as soon as the ADJUSTMENT counter reading becomes zero.

(B) If no borrow was obtained,

(a) the ADJUSTMENT counter reading is tested. If it is found to be zero, no lining-up is needed. If, however, it is non-zero, then

(b) S.R. is shifted left and one pulse per each shifting is entered into the ADJUSTMENT counter (counting down) as well as the AUGEND counter (counting up). The shifting is discontinued as soon as the ADJUSTMENT counter reads zero.

(v) Same as (v) in CASE I.

(vi) Same as (vi) in CASE I. Also, in addition, (c) the STORAGE counter is disabled and its content is jam transferred into the ADJUSTMENT counter.

CASE III - PRODUCT ACCUMULATOR ON - FIRST "=+" in course of the operation:

(i) to (v) - Same as in CASE I.

(vi) The carry obtained in (v), (a) clears S.R. and M.S.R., (b) clears both the AUGEND and the ADDEND counter and sets the ADJUSTMENT counter to count down, and (c) makes STORAGE counter ready to count up.

(vii) S.R. reads-in the content of P.R.

(viii) An ADDITION/SUBTRACTION CYCLE is initiated so that the content of S.R. is added to the content of ST.R. At the end of the cycle, a carry is generated from COUNTER 2.

(ix) The carry obtained in (viii), (a) clears S.R. and M.S.R., (b) removes the blanking on the display and (c) makes S.R. ready to take in the next entry.

CASE IV - PRODUCT ACCUMULATOR ON - SECOND AND SUCCESSIVE "=+" in course of the operation:

(i) to (v) - Same as in CASE II except for the following change in step (iv):

In step (b) of CASE (A), ST.R., instead of P.R., is shifted left.

(vi) - Same as (vi) in CASE III. Also, in addition, (d) disables the STORAGE counter and jam transfers its content into the ADJUSTMENT counter.

(vii) to (ix) - Same as the corresponding functions in CASE III.

12. "=-" - Same as that for "=+", only change being that in step (i), the P.R. is set to count down.

13. "÷" - (i) It is checked whether the divisor, stored in S.R., is zero. If it is zero, then the process of division is not carried out at all and the OVERFLOW INDICATING RED LAMP is lighted. If, however, it is not zero, then

(ii) The P.R. and the QUOTIENT counter are set to count down.

(iii) The display is connected to M.S.R. and is blanked. Its decimal point is set to be read from the DIGITS counter.

(iv) Lining-up - Now the two operands are lined up by the same process as described under SECOND "+" of "+" key (in this Section); however, the following minor additions have to be incorporated:

(A) (a) The DIGITS counter is also set to count up.

(b) One pulse per each shifting is also entered into the DIGITS counter (counting up).

(B) (b) One pulse per each shifting is also entered into the DIGITS counter (counting down).

(v) At the end of the lining-up operation, a pulse is entered into the QUOTIENT counter.

(vi) "Digit equalling" - The DIGITS counter reading is tested. If it is "negative" (i.e., has a standing borrow, e.g. 7, 8 etc.) no digit-equalling is needed and the machine directly goes to step (viii) below.

If the DIGITS counter reading is non-zero and "positive" (i.e., has no standing borrow, e.g. 1, 2, etc.), digit equalling is necessary and is carried out by the same method as described in Section 4.3.4 under the "÷" key. However, if the DIGITS counter reading is zero, no digit equalling is needed and the machine goes to the next step.

(vii) Now, a DIVISION CYCLE, described in Section 4.3.4 and a little modified as shown below, is carried out.

Modifications: (a) In step (ix) (a): No pulse is entered into the M.S.R. and instead, a pulse is entered into the QUOTIENT

counter (counting down).

(b) In step (xii): If the CHECK counter reading in step (x) is a zero, then the machine goes to the next step [i.e., step (viii), described below] , instead of removing the blanking of the display.

(viii) The DIGITS counter is reset and is made to read-in the content of the QUOTIENT counter.

(ix) The reading of the QUOTIENT counter is tested for zero. If it is zero, the machine goes directly to step (xi). If, however, it is non-zero, then

(x) (A) The P.R. and M.S.R. are shifted one place to the left.

(B) An ADDITION/SUBTRACTION CYCLE is initiated so that the divisor (in S.R.) is subtracted once from the dividend (in P.R.). At the end of the cycle, a carry pulse is given out by COUNTER 2.

(C) If no borrow was obtained from the P.R. in step (B), the carry pulse is entered into M.S.R. to count it up and the step (B) is repeated.

(D) The cycle comprising steps (B) and (C) is repeated so long as no borrow is obtained from P.R. in step (B).

(E) If a borrow is obtained from P.R. in step (B), (a) no pulse is entered into M.S.R. and instead, a pulse is entered into the QUOTIENT counter (counting down), (b) the P.R. is set to count up, and (c) an ADDITION/SUBTRACTION CYCLE is initiated so that the content of S.R. is <u>added once</u> to the content of P.R. At the end of (c), a carry pulse is given out by COUNTER 2.

(F) When the carry pulse is obtained at the end of step (E), (a) the P.R. is set to count down and (b) the QUOTIENT

counter reading is tested for zero.

(G) If the QUOTIENT counter reading in step (F) is non-zero, (a) the P.R. and M.S.R. are shifted one place to the left and (b) the steps (B) through (F) are repeated.

If, however, the QUOTIENT counter reading in step (F) is zero, the machine goes to the next step.

(xi) The whole process of DIVISION is now deemed to have been completed with the quotient stored in M.S.R. and the remainder retained in P.R. The blanking of the display is removed so that the M.S.R. is displayed; also P.R. is cleared.

14. "RESTORE" - Same as listed in Section 4.4.

15. "SUM" - (i) The display is connected to S.R. and is blanked. Its decimal point is set from the STORAGE counter.

(ii) The content of the ST.R. is tested. If it is "positive" (i.e., no borrow was obtained from the ST.R. during the accumulation of the last product), then the machine directly goes to step (viii). If, the ST.R. reading is "negative" (i.e., in complement form), then

(iii) The ST. R. is set to count down.

(iv) The negative cathode of the NIXIE tube for sign display is connected in place of the positive cathode.

(v) S.R. reads-in the content of ST.R. and ST.R. is cleared.

(vi) An ADDITION/SUBTRACTION CYCLE is started to subtract the content of S.R. from that of ST.R. (i.e., 0) and it gives out a carry from COUNTER 2.

(vii) The carry thus obtained clears the S.R. Also,

(viii) S.R. reads-in the content of ST.R. and the blanking on the display is withdrawn so that S.R., storing the sum, is displayed.

CHAPTER - VII

7.1 WHAT HAVE BEEN DONE AND WHAT COULD NOT BE DONE:-

In the preceding Chapters, after a review of the various types of desk calculators, their component parts and method of working (Chapter I), a complete system and logical design together with a detailed study of other important aspects were presented for a small five-digit machine with integer mode operation (Chapters II, III & IV). In Chapters V & VI, a method of achieving automatic decimal point adjustment during the various integer mode operations was suggested and the ideas developed in the previous Chapters were incorporated and extended to the design of a "more sophisticated desk calculator" with ten-digit capacity, floating point operation and the capability of executing a few additional operations.

It has not been possible to make a significant headway into the aspect of hardware realisation owing to limited time and largely because of the same reason a minimal logic design cannot be claimed to have been achieved. The presentation, on the whole, may sometimes appear to be much too elaborate but it may be justified in the light of the fact that the present work presents the preliminary ideas for the Desk Calculator Project undertaken by the Electrical Engineering Department at the Indian Institute of Technology, Kanpur.

7.2 COMMENTS ON THE COST AND COMMERCIAL MODEL:-

The total component cost for the small machine was

estimated as Rs.19,000.00. The same, when extrapolated for the "more sophisticated model", leads to a cost estimate of approximately Rs.35,000.00. This appears prohibitively high to recommend the model for commercial manufacture. However, by developing an indigeneous display system, doing away with D-C-D gates, minimising and simplifying the logic design, adopting mass production techniques and finally, economising on the quantity as well as quality of the components the cost can be easily brought down to something between fifteen to twenty thousand rupees for the sophisticated model and around ten thousand rupees for the five-digit model. Another interesting fact observed is that the introduction of floating point arithmetic is not at all expensive and hardly adds Rs.1500.00 to the cost for integer mode operation.

Commercially available desk calculators offer some additional features and facilities over those contemplated for the "more sophisticated model" discussed in Chapter V. However, a fact is clearly brought out that many an additional feature can be introduced in the proposed model by slightly modifying the machine functions corresponding to different keys in a judicious manner; this will, admittedly, complicate the control logic but it is felt that it will add negligibly to the cost.

7.3 SOME OBSERVATIONS AND SUGGESTIONS:-

It is feasible to manufacture electronic desk calculators under the prevalent conditions of the electronic industry in the country, using the present design; however, the cost seems to be

large mainly because of the high cost of the presently available switching transistors which have been used for shift registers (memory). Thus it may be worthwhile to explore the possibility of using some other type of shift registers, e.g., delay line, in an attempt to bring down the cost. On the other hand, it is possible that the cost of shift registers may be greatly reduced in future with the advent of integrated circuits in India.

It is quite obvious that in order to successfully achieve the aim of the desk calculator project, a good amount of work is required to be done; a few important ones are suggested below:

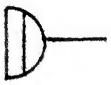
1. Develop a cheap and simple indigeneous display system.
2. Improve upon the input system and logic design, suggested in this report.
3. Prepare a digital computer programme to check the validity of the logical design for the small machine.
4. Try out delay line memory as a substitute for flip-flop storage.

APPENDIX A - SYMBOLOGY

Standard logic level

Standard pulse

D-C-D gate



AND gate

OR gate

S-R flip-flop

Monostable Multivibrator

Delay

S P D T relay normally open

APPENDIX B - BIBLIOGRAPHY

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